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Electrical and surface characterization for InAs/GaAs site-controlled Quantum Dots in Schottky diodes

Master of Science Thesis

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PREFACE

This Master of Science's Thesis is conducted in collaboration between the department of Electronics and the Optoelectronics research centre at Tampere University of Technology.

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ABSTRACT

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Major subject: C-V measurements in Schottky diodes, surface characterization.

Keywords: C-V measurements, Schottky diodes, Site-controlled Quantum dots, QCA, AFM, SEM, EBL, Chemical cleaning, Etching, double pits.

In this thesis, a research study is held as a part of the Photonic quantum cellular automata (PhotonicQCA) project at the Tampere University of Technology. The study includes both surface and electrical characterization for the site-controlled quantum dots (QDs). The surface characterization includes the statistics of the pits diameter. The statistics shows that for 30 and 40 nm pits, the occupational probability with QDs is low. The best case is obtained with 50 nm. Additionally, the problem with 60 nm pits was due to filling the pit with multiple QDs. Thus, 50 nm diameter pits were selected for the project. The research work in the thesis continues to study the double pits with different spacing and orientation. The aim of the study is to find out which orientation and spacing shall fulfil the needs of the project. The study includes three orientation; [011] double pits, [0-11] double pits, and [010] cross double pits. For each orientation, 10 different spacing's between the pits are studied from 45 to 100 nm. The [011] orientation affords the minimum spacing between the pits. Additionally, the spacing between the two QDs (after the pits are filled) increases steadily with the increase of the distance between the pits.

The electrical characterization of the QDs is performed in Schottky diode structure where the capacitance is measured as a function of reverse applied voltage at different temperatures. There are 9 samples which are involved in the study. The samples are prepared in a way to observe the effect of each fabrication step on the overall capacitance. Due to the chemical cleaning step which is needed before the sample is loaded to the Molecular beam epitaxy reactor, a remarkable defect layer is created which trap the electrons and screen the depletion region. Thus, the capacitance does not change normally with the applied voltage and the site-controlled QDs layer does not contribute to the overall capacitance which is kept constant until the depletion layer pass over this parasitic defect layer.

ABBREVATIONS

AFM	Atomic force microscopy
CAR	Continuous azimuthal rotation
CDP	Cross double pits
C-V	Capacitance-Voltage
EBL	Electron beam lithography
FTDS	Fluorodecltrichlorosilane
HDP	Horizontal double pits
ICP	Inductively coupled plasma
IPA	Isopropyl alcohol
MBE	Molecular beam epitaxy
MIBK	Methyl isobutyl ketone
ML	Monolayer
MOVPE	Metalorganic vapour phase epitaxy
NIL	Nanoimprint lithography
ORC	Optoelectronics research centre
PDMS	Polydimethylsiloxane
PL	Photoluminescence
PMMA	Polymethyl methacrylate
QCA	Quantum cellular Automata
QD	Quantum dot
QDD	Quantum double dot
QW	Quantum well
RGB	Regrowth buffer
RHEED	Reflection high energy electron diffraction
RIE	Reactive ion etching
SEM	Scanning electron microscopy
SK	Stranski-Krastanov
SQCA	Semiconductor QCA
TUT	Tampere University of Technology
UV-NIL	Ultraviolet-NIL
VDP	Vertical double pits
WL	Wetting layer

SYMBOLS

ϕ_m	Metal work function
ϕ_s	Semiconductor work function
χ	Electron affinity
ϵ_o	Absolute permittivity
ϵ_s	Relative permittivity of silicon
ρ_{QD}	Negative charge density due to the filled electron states in those QDs
x_{QD}	Distance of the Quantum dot layer from the schottky contact
A	Surface area
C	Capacitance
C_∞	Capacitance at equilibrium
E_C	Conduction band energy level
E_F	Femi energy level
N_d	Donor concentration
n_{QD}	Electron density in the QDs layer
N_{QD}	Density of the QDs
$n(w)$	Doping density level
V_o	Contact potential
V_o	Bias voltage
$V(x)$	Potential difference
w	Width of the depletion region
w_∞	Depletion region width at equilibrium

1. INTRODUCTION

For the last two decades, the complementary metal-oxide semiconductor (CMOS) technology has been the only industry standard for all integrated devices. One alternative for the CMOS is the Quantum cellular automata (QCA). Theoretically speaking, QCA can operate in the order of the terahertz frequency with remarkably low power consumption. The research has recently focused on different types of QCA; metal, magnetic, molecular and semiconductor QCA. As a part of the PhotonicQCA project in TUT, the aim is to find out if it would be possible to fabricate a photonicallly excited QCA cell.

The thesis discusses generally about the difference between the self-assembled and the site controlled Quantum dots (QDs) before it gives an overview about the fabrication process for the InAs/GaAs site-controlled QDs including; the lithography, the etching and growth. Both Electron beam (EBL) and Nanoimprint lithography (NIL) are discussed. Additionally, the thesis presents two different surface characterization methods which have been involved in the study; Scanning electron microscopy (SEM) and atomic force microscopy (AFM). It is also shown how it was possible to use them for the study. Additionally, a theoretical background has been presented discussing about the Schottky diode especially the Schottky diode structure with embedded QDs layer.

The thesis gives an introductory study for the surface and electrical characterization of the site-controlled QDs. It includes some statistics to find out which diameter has to be used for the pit in order to be filled with a single QD. Another study for the double QDs (two QDs which are closely separated) is also involved in order to reveal what could be the suitable orientation and distance between them in order to fulfil the requirements for the project. Finally, for the electrical characterization, the aim is to discuss about the C-V curve for those Schottky diode structures and how the fabrication process shall affect on the overall capacitance of the structure. In the end, a conclusion is added to summarize the findings and the results of the thesis.

2. BACKGROUND THEORY

The aim of this section is to explain the background of topics which are involved in the thesis. The first part discusses about the theory of the QCA and how it is possible to use the QCA technology in order to manufacture logic circuits with extremely low power consumption in the future. Furthermore, the second part gives different information about the site-controlled QDs: applications, fabrication and position control. Finally, there is a discussion about the Schottky diode structures and operations which is used in this research work.

2.1. Quantum Cellular Automata electronics

QCA's were one of the most promising nanotechnologies proposed in the early 90s by P.D. Tougaw in the field of electronics. In this technology, a QCA-cell, as shown in figure 2.1, is the basic structure for the circuit implementation. It is claimed – both theoretically and experimentally – that the QCA circuits can be operated in THz frequencies with low power consumption [1]. A QCA cell contains 4 QDs of which two are charged with electrons while the other two QDs are kept empty. The relative positions of the electrons inside the QDs define the state of the QCA cell. Figure 2.1 shows a QCA cell in the two different possible states. The challenge is to excite and to move an electron from one dot to another.

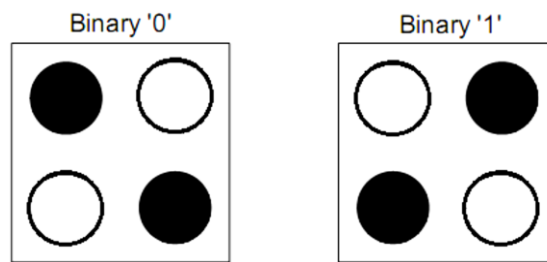


Fig. 2.1: QCA cell in the different possible states: 0 and 1.

By moving an electron horizontally from the upper QD to the adjacent one, then an electron from the lower filled QD shall move to the lower neighbouring QD, as shown in Fig. 1.1. This happens due to the Coulombic interaction between the electrons [2].

One simple QCA application can be the QCA wire which is shown in Figure 2.2. If one electron moves from one dot to another, the effect will continue through the whole wire. Thus, the state will be interchanged at the end of the QCA wire as well. Also there are

more different structures which can be implemented using QCA cells. For example; AND gate, OR gate and NOT gate [2].

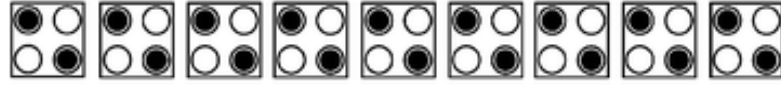


Fig. 2.2: QCA wire contains several QCA cells [2].

There are many ways to fabricate a QCA cell like: metal, semiconductor, magnetic and molecular QCA cells. In metal QCA, QDs are made of metal like aluminum and they are connected to each other through oxide tunnel junctions and capacitors. Furthermore, in the magnetic QCA, the magnetic field is used to control the nanoparticles which create bistable system [3].

The semiconductor QCA (SQCA) is fabricated by using InAs/GaAs heterostructure with a high mobility 2-dimensional electron gas below the surface of the substrate. An Au/Ge/Ni alloy is evaporated to make an ohmic contact to the electron gas underneath. Finally, using optical and EBL patterning beside metal evaporation, Ti/Au surface gates shown in figure 2.3 are created. The main problem with the SQCA is that they can only operate at 60 mK temperature [4].

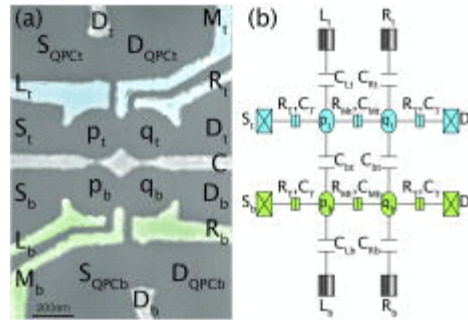


Fig. 2.3: AlGaAs/GaAs SQCA based on 2DEG operating at 60 mK.

One aim of the PhotonicQCA project in the TUT is to fabricate a SQCA using another approach which allows the operation of the QCA cell at higher temperatures; in K range instead of mK. The study is related to the growth of site-controlled InAs QDs (SCQD) on a patterned GaAs substrate where the QDs are grown into the pre-patterned surface (etched holes in this case).

As part of the PhotonicQCA project, this master thesis is concerned with one aspect related to the growth of the QDs. One has to choose a suitable diameter of the etched holes (pits) containing the QDs and a correct spacing between the QDs in order to facilitate the transition of electrons from one QD to another when it is excited through light. Figure 2.4 shows an SEM image taken at the Optoelectronics research center (ORC)

clean rooms for 8 site-controlled QDs. The process for the fabrication of the QDs is discussed later on Section 3.1.

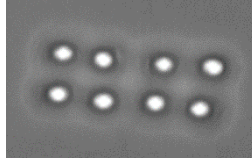


Fig. 2.4: SEM image of 8 Site-controlled QDs image.

2.2. Site-controlled quantum dots

Since the semiconductor Quantum dots (SCQDs) are the building block for the SQCA technology, it is necessary to have a quite enough understanding about their characteristics and how to control their position during fabrication.

QDs are typically fabricated by epitaxial growth methods. The epitaxial growth means that the crystal structure of the substrate is reproduced into the next layer by depositing atoms of the desired elements on the surface. In QD growth, the difference in the lattice constant between the substrate and the QD materials leads to a strain which is relieved by the formation of 3-dimentional islands which basically decreases the surface energy [5]. The most common reactor types used for the epitaxial growth are the MBE and the metalorganic vapour phase epitaxy (MOVPE). For this thesis, only the MBE reactor in the ORC is used for growing the samples discussed in section 3.3.

There are two types of QDs growth: self-assembled and site-controlled QDs. In the self-assembled QDs, the QDs are randomly positioned on the substrate. The QDs are typically between 20 to 40 nm in diameter and up to 15 nm in height. Stranski-Krastanov (SK) growth mode is used to growth InAs QDs on GaAs substrate. In SK growth mode, a 2-dimentional layer of InAs whose thickness is a couple of monolayers (ML) – often called wetting layer (WL) – is formed first on top of the GaAs substrate before the formation of the 3-dimentional QDs [6] as shown in Figure 2.5. Figure 2.6 shows an AFM image of self-assembled InAs QDs on GaAs substrate [5] [7].

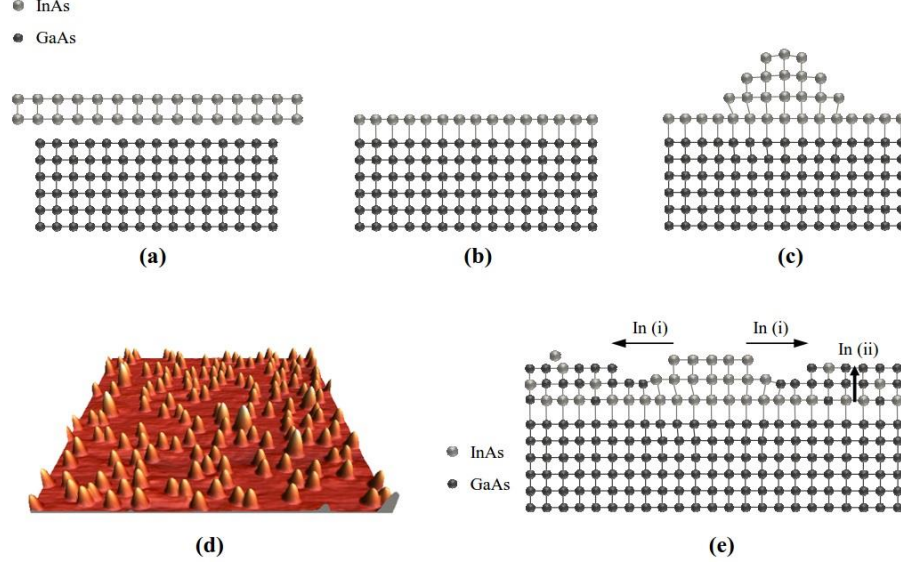


Fig. 2.5: InAs QD growth process on GaAs substrate. (a) Shows the InAs ML and GaAs surface at equilibrium. (b) Formation of a 2-dimensional WL on GaAs surface. (c) InAs accumulation forming 3-dimensional island when the critical thickness is reached. (d) $1 \times 1 \mu\text{m}^2$ 3-dimensional AFM image of InAs/GaAs SQDs with density around $1 \times 10^{18} \text{ cm}^{-2}$. (e) The height of the QD is decreased due to the migration of the InAs atoms from the upper part of the QD to the surface of the GaAs in addition to the InAs atoms which set apart from the WL to the GaAs surface [7].

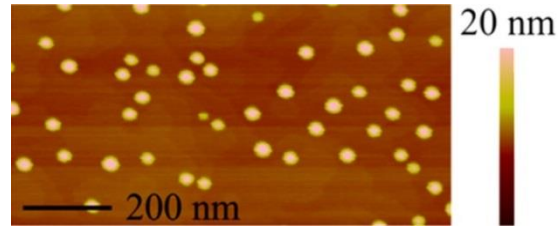


Fig. 2.6: 2-dimensional AFM image of self-assembled InAs QDs grown on GaAs substrate [5].

However in order to make the QDs more suitable for advanced applications, it is beneficiary to control its position. Thus, one shall control its optical and electrical properties. In the site-controlled SK growth, the nucleation locations are defined by lithography and etching process [8]. One way to do the patterning is the EBL which is used to define those nucleation locations before they are dry-etched into small pits [9] [10] [11].

For the PhotonicQCA project, EBL based patterning process has been used to define those nucleation locations of the grown QDs. Figure 2.7 shows a schematic diagram of the site-controlled QD growth process including the adsorption, desorption and migration of In atoms on the GaAs surface. Additionally, figure 2.8 shows AFM and SEM images for the site-controlled InAs/GaAs QDs.

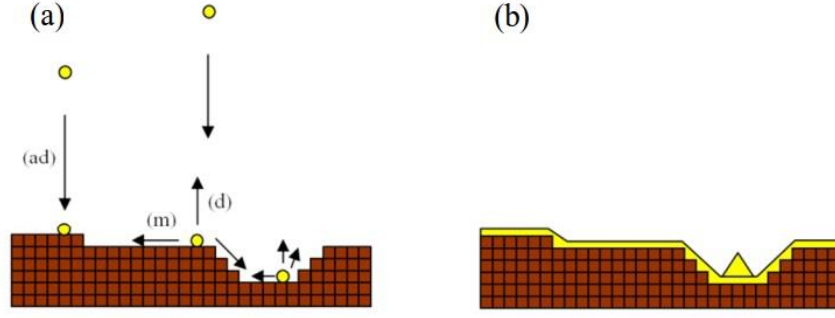


Fig 2.7: (a) Indium atom adsorption (ad), desorption (d) and migration (m) on GaAs surface. (b) 2-Dimensional WL of InAs and QD formation inside the pit [5].

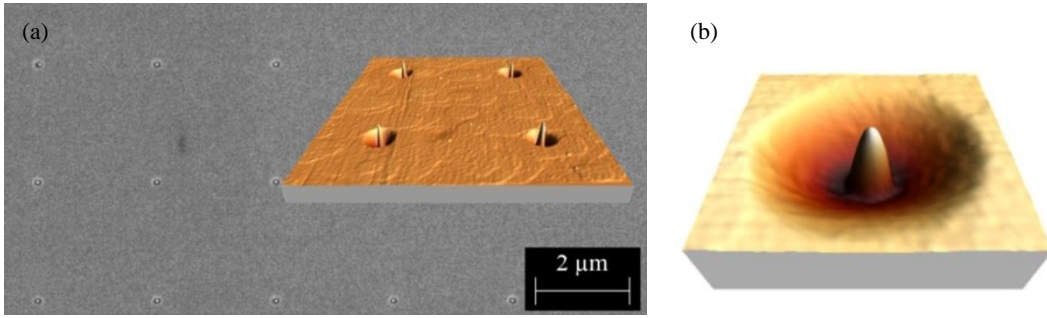


Fig 2.8: (a) SEM and AFM images of an array of single site-controlled QD with period of 2.5 μm and diameter of 100 nm. (b) AFM image of a Site-controlled QD in pit whose diameter is 250nm [7].

2.3. Schottky Diode

Furthermore, as part of the PhotonicQCA project and in this thesis, GaAs Schottky diodes with embedded site-controlled InAs QDs are studied. The Schottky diode is a metal-semiconductor diode which can be fabricated by simply depositing a metal over a semiconductor to form a metal-semiconductor junction. Schottky diodes have gained a lot of interest due to its simplicity in the fabrication. Additionally, they are very useful in high speed applications in general and specifically in fast rectify applications [12].

In order to remove an electron from the Fermi level of the metal to the vacuum, the electron must have an energy equal to $q\phi_m$ which is called the metal work function which is different from one metal to another. When a metal with work function $q\phi_m$ is deposited on a semiconductor which has a work function of $q\phi_s$, a charge transfer process occurs and continues until the two Fermi levels align together as shown in Figure 2.9. The figure shows the Fermi level alignment for an n-type semiconductor whose Fermi level is higher than the Fermi level of the metal. The electrostatic potential of the semiconductor is raised relative to the one of the metal. The depletion region W is formed inside the semiconductor. The positive charges due to the uncompensated donor ions within the depletion region shall equal to the positive charges on the metal.

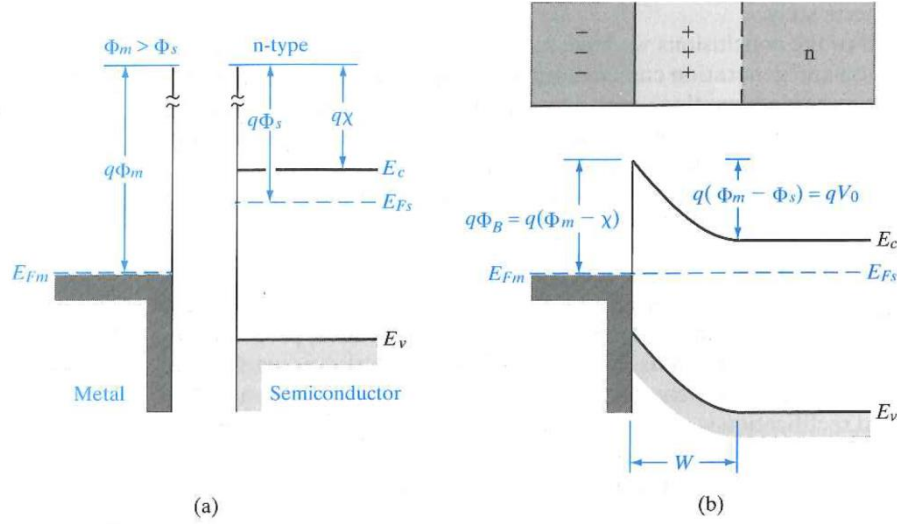


Fig 2.9: Schottky diode of a metal and an n-type semiconductor whose Fermi level is higher than the Fermi level of the metal (a) the band diagram before alignment. (b) Band diagram after the alignment (at equilibrium).

The electron affinity $q\chi$ is measured from vacuum level to the conduction band of the semiconductor. It is used to define the potential barrier for the electron injection from the metal into the conduction band of the semiconductor $q\phi_B$ [12]. The equilibrium contact potential qV_o is formed due to the difference between the metal and the semiconductor work function. It prevents further electron diffusion from the semiconductor to the metal. It can be written as

$$qV_o = q(\phi_m - \phi_s) = q\{\phi_m - (\chi - [E_C - E_F])\}. \quad (2-1)$$

The potential difference can be reduced or increased by applying forward or reverse bias voltage depending on the application.

In order to calculate the width of the depletion region, one can easily assume that the metal is a heavily p-type doped semiconductor. Thus, the situation would be similar to p^+n junction. Thus, it can be calculated from the solution of the poisson's equation in the depletion region. The width of the depletion region can be calculated as:

$$W = \sqrt{\frac{2\epsilon_o\epsilon_s}{qN_d} (V_o - V_b)}, \quad (2-2)$$

Where V_b is the applied bias voltage, the N_d is the donor concentration.

Figure 2.10 shows the depletion width variation with respect to the reverse voltage applied for an n-type GaAs semiconductor Schottky diode for different concentration lev-

els. The doping level varies from 10^{15} to 10^{17} cm^{-3} . It is noticed with low charge concentration and high reverse bias; one shall obtain the largest depletion width [13].

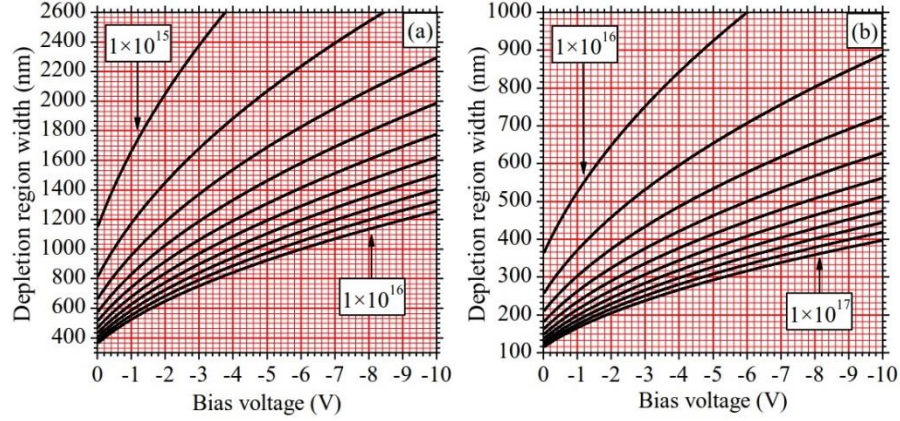


Fig. 2.10: shows the depletion width of n-type semiconductor in Schottky diode as a function of the bias voltage as well as the doping concentration [13].

The depletion capacitance can then be calculated as:

$$C = \frac{\epsilon_o \epsilon_s A}{W}. \quad (2-3)$$

As shown in (1-3), the depletion capacitance is reversely dependant on the depletion width. Thus, it is possible to observe the capacitance value change with the bias reverse voltage in order to understand the variation of the depletion width as will be shown later in section 3.4.

The previous discussion in this section was related to Schottky contact in which there is an intention to have a depletion region inside the semiconductor material. The Schottky contact is often used in rectifying the signal. On the other hand, for some application, it might be required to have a metal-semiconductor contact with minimal resistance. In such contact, it is required not to rectify the passing signal. This type of contact is called an ohmic contact. In order to fabricate an ohmic contact, for example in n-type semiconductor Schottky diode, the Fermi level of the semiconductor has to be lower than the Fermi level of the metal. Unlike the Schottky contacts, there is no depletion region in the semiconductor part of the diode. One practical way to create ohmic contact is to dope the semiconductor material heavily in the contact region. The barrier layer between would be small enough to allow the charges to tunnel through it from the metal to the semiconductor. Figure 2.11 shows an ohmic contact for an n-type semiconductor after and before the equilibrium [12].

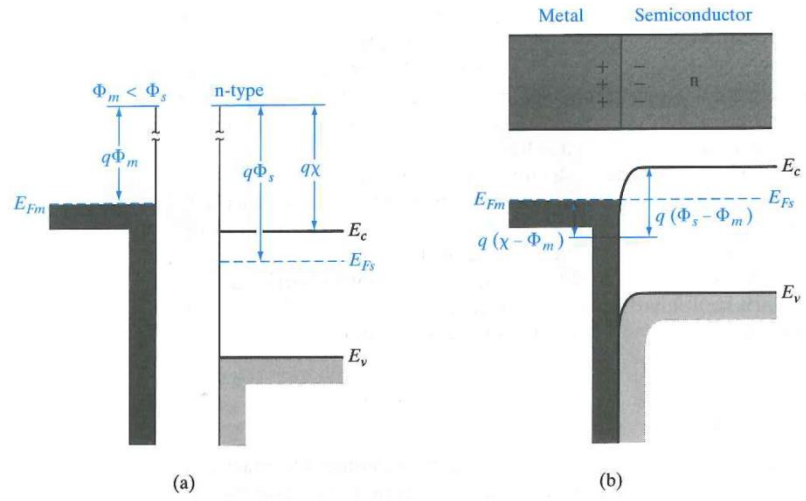


Fig. 2.11: Ohmic contact for n-type semiconductor (a) before equilibrium with $\phi_m < \phi_s$. (b) Equilibrium case after Fermi level alignment [12].

3. SAMPLE PREPARATION AND CHARACTERIZATION

The aim of this chapter is to show the preparation process of the different samples used in the QCA project. There were two different samples which were studied in this thesis. The first samples were fabricated in order to find out the most suitable diameter for the pits. Each pit has to be filled with only one QD. Additionally, the spacing and the orientation for each two double pits are varied and studied. In such sample, many processing steps have been carried out, for example: spin coating, electron beam lithography, mask development, dry etching and chemical cleaning.

On the other hand, a study on different samples is carried out in order to check the effect of these various processing steps, such as patterning, chemical cleaning and the QD layer growth on the electrical properties of those samples. Additionally, the MBE growth factors and parameters are discussed.

Furthermore, a brief discussion is about AFM and SEM. Both have been used to perform the surface characterization of the EBL samples. Some other data is also presented about the Schottky diode structure and the C-V measurements for the NIL samples.

3.1. Fabrication process

In this section, the fabrication process of the two different samples is explained in details. The main difference in the fabrication process between the EBL and the NIL sample types is the lithography technique used. The nanoimprint lithography (NIL) is used for the samples whose C-V graph is measured. By using NIL, large area on the wafer could be patterned at once with it. For the site-controlled QD samples, in which sparsely located sub-100 nm features were required, EBL was used instead of the NIL. Sparse patterns are difficult to make with the NIL as shown later in the results chapter.

3.1.1. Nanoimprint lithography Process

The first step in the lithography process is the spin coating of the resist on top of the sample surface. Firstly, the sample is cleaned and prebaked in order to remove the moisture from the sample surface. Moisture on the wafer surface can cause poor results in the spin coating and lithography process. In the pre-bake, 120 °C was the temperature

used for 2 minutes on a hot plate. The sample is then let to cool down before the spin coating step [16].

For the NIL samples, mr-UVCur06 was used as a resist [17]. During the spin coating, the centrifugal force – when the substrate spins with several 1000 rounds per minute (rpm) – shall distribute few milliliters (ml) of resist over the surface of the substrate. The viscosity of the material as well as the rotational speed of the spinner controls the thickness of the photoresist layer.

The sample with dispensed resist was rotated with 1500 rpm in a closed chamber for 20 s. The thickness of the photoresist layer is around 50 nm. After coating, the resist shall contain a small amount of remaining solvent which is removed by baking it at the 80 °C on the hot plate. The sample is baked in order to decrease the remaining solvent and to avoid mask contamination and sticking to the mask. Figure 3.2 shows the image of the spinner machine used for spin coating the sample at ORC's clean room.



Fig. 3.2: the spinner Coat ST 23+ manufactured by OPTI used for spin coating the samples in this thesis.

In the NIL, designed master templates are used to fabricate stamps which are needed to transfer required micro and nanoscale patterns into the resist and even further into the wafer. There are two types of NIL, the thermal NIL and the ultraviolet-NIL (UV-NIL) [16]. In the thermal NIL, the heat is used to harden the resist to the shape of the stamp. On the other hand, for the UV-NIL it is the UV-radiation which hardens the resist. The most beneficiary advantage for the NIL is that it can replicate the nanoscale patterns in a very cheap and fast way over large areas. It has been proven that it can be adapted for QDs arrays as in [17]. For that reason the NIL has been involved in the fabrication of the Schottky diode samples with embedded QDs layer inside.

There are two types of NIL stamps: hard and soft stamp. Hard stamps can be made from silicon or SiO_2 . Hard stamps don't change their shape or bend, thus it would be very sensitive to the cleanliness of the substrate surface. Any particle on the surface of the substrate will cause an insufficient contact between the stamp and the resist. On the other hand, soft stamps made of polydimethylsiloxane (PDMS) – a polymeric compound which contains silicon – are more flexible and the stamp will adapt to those defects. There will be few local defects in the pattern at some locations where those unwanted particles exist. However, the overall patterning would be successful [18].

Figure 3.3 shows the schematic structure for the used stamp. It contains a support layer made of thick glass wafer. The layer beneath – which works as a flexible buffer layer – is made of the soft-PDMS. Finally, a thin rigid glass layer which contains the patterned layer made of Ormstamp material lies at the bottom [18] [19]. Figure 3.4 shows the patterns in the master mold used in this thesis.

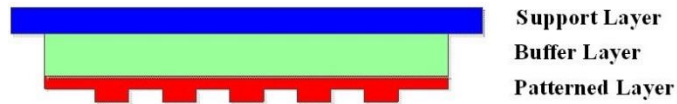


Fig. 3.3: Stamp construction showing its 3 different layers [20].

A master mold is always needed in order to fabricate the stamp. It has the same exact pattern needed to be patterned on the resist. The master mold is often fabricated from silicon (Si) due to its availability, price and processing properties. Additionally, Si is commonly used in the semiconductor technology process and thus the etching processes are well known. Furthermore, the EBL is mostly used to pattern those master molds. The PDMS master molds which are used in thesis are always coated with anti-adhesive perfluorodecyltrichlorosilane (FDTS) in order to make it easier to release the stamps from the masters and to keep the masters as clean as possible.

Figure 3.4 shows an SEM image of the master mold which has been used in the fabrication of the site-controlled QDs layer in the Schottky diode NIL samples.

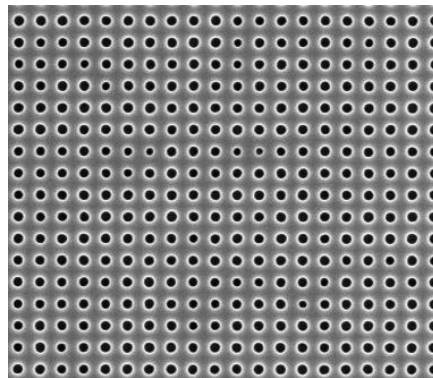


Fig. 3.4: The master mold used to fabricate the QD layer for the C-V measurements samples.

For the NIL process, EVG620 lithography system shown in Figure 3.5 is used. It is basically an optical lithography system with an add-on NIL tool. The NIL process is done in vacuum conditions in order to remove bubbles from the resist. The stamp and the sample with resist are attached to the stamp holder and chuck using the vacuum. The stamp and sample are aligned and are brought close to each other. When the vacuum is applied to sealed chamber, the stamp and the sample become in contact. It takes some time until the resist fills the patterns in the stamp. Next, the UV light is used to harden the resist. For this thesis, mr-UVCur06 resist was used, which had to be exposed for 3 minutes. The stamp is detached from the master by slowly bending from the corner of the stamp [18].

However, the main issue with the NIL is the residual layer – or bias layer – which always appears at the bottom of the pattern at the surface of the wafer after imprinting. Thus, the resist layer must be matched to the fill factor of the pattern in order to minimize the thickness of the bias layer. The residual layer can be removed by reactive ion etching (RIE) with short O_2 plasma step.

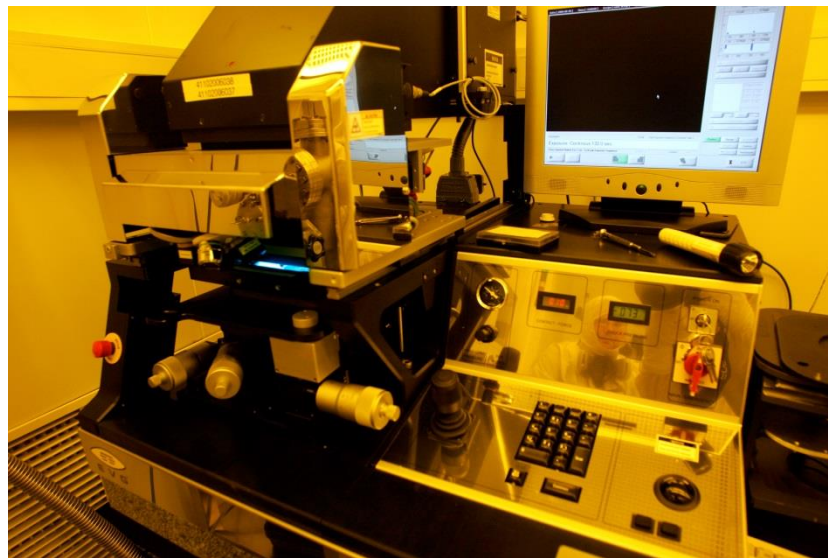


Fig 3.5: the EVG620 system used for the NIL process in this thesis.

Figure 3.6 shows the basic process steps which are used for the NIL. It includes the master fabrication, stamp casting and separation, spin coating of the wafer, the imprinting and the hardening the resist using the UV. Finally, the sample should be ready for etching.

Anisotropic dry etching is the key factor for making small QDs since it is hard to control the wet etching in lateral direction. Thus, dry etching has been used for both samples; the NIL and the EBL samples. For this thesis, two dry etching systems are used; reactive ion etching (RIE) and the inductively coupled plasma (ICP). The selection between these two systems depends on the available etching gasses in each system and

etching profile requirements. In the ORC's clean room, there is a policy to etch polymers, dielectrics and other Freon-based etchings in the RIE. On the other hand, semiconductor etchings with chlorine-based chemistries are done using the ICP. The policy has been used in ORC in order to avoid contamination of the chamber due to Freon and chlorine intermixing.

For the NIL samples discussed in this section, GaAs substrate was etched using ICP-RIE, the BCl_3/Ar recipe which was applied for 13-16 seconds. The used etching parameters were, 20 Watt RF power, 4.5 mTorr pressure and 300 Watt ICP power in addition to having the liquid nitrogen cooling at 25°C . Next, the sample was etched again for 10 minutes in the RIE O_2 plasma with 100 mTorr pressure and 100 Watt RF power in order to remove the remaining NIL resist layer.

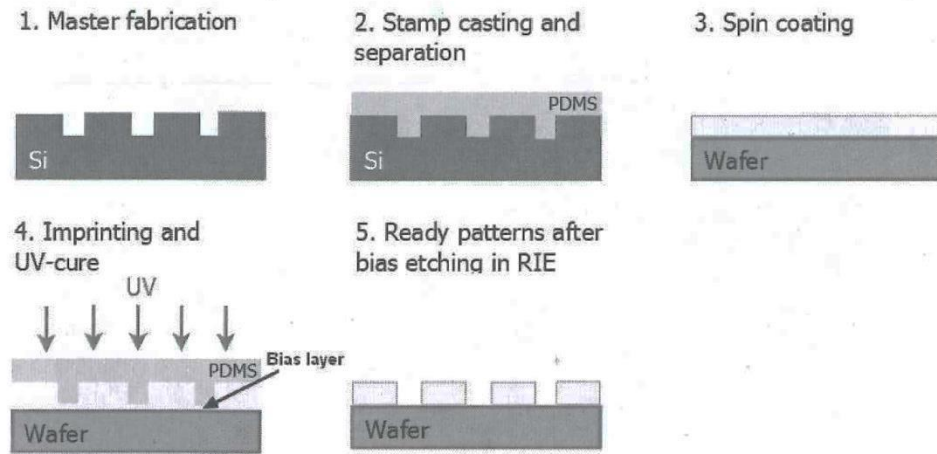


Fig. 3.6: The basic process step involved in the NIL [18].

In addition to the previously discussed problems with the NIL, there was a major problem with the imprinting of small sized and sparsely distributed patterns. Those patterns were needed for optimizing the size and spacing between the pits to allow the electron transfer between them. In the research done in reference [18] the master mold with 50, 100 or 150 nm holes and periodicity between 500 nm and $10\ \mu\text{m}$ was used with a lot of difficulties. Sparsely located small patterns were squeezed during the imprint process. The 100 nm and 150 nm pits were printed; however they had a wider diameter with about extra 50 nm. Additionally, the 50 nm pits were not imprinted at all [18].

For such reasons, the EBL was used instead of the NIL for processing those samples. Figure 3.7 shows how the 100 nm diameter holes got wider and were distorted. The spacing between the pits is $2\ \mu\text{m}$. However by using EBL, as will be shown in chapter 4, the minimum pits size went down to 5 nm without any limitation regarding to the spacing between those pits. On the other hand, the EBL which requires more infrastructures and the lithography system is more complex than NIL [22].

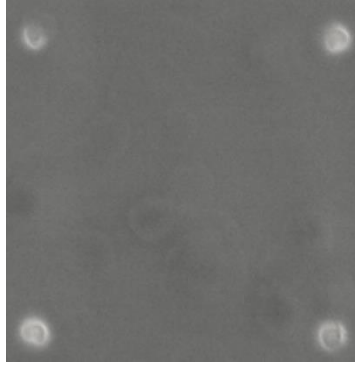


Fig. 3.7: Distorted and widened pits processed by NIL. The diameter is found to be 150 nm instead of 100 nm. The spacing between every two dots is 2 μm in both the horizontal and the vertical direction.

3.1.2. Electron beam lithography

The aim of this part is to discuss about the EBL background as well as lithography process steps for patterning the samples used in this thesis.

EBL is based on exposing the resist, which in this case is PMMA, with highly focused and narrow beam of electrons which are accelerated with a high voltage. The electron beam causes fragmentation of the PMMA polymer chains and thus it will turn into smaller molecular parts. The process is known as chain-scission. Those areas which are exposed and fragmented can then be easily removed by a suitable developer [23]. The diffraction limit is the theoretical limitation of the EBL resolution which depends on the electron wavelength, i.e. the energy. However, the electron diffusion and scattering in the photoresist are the limitation for the resolution [24]. The EBL machine must be located in a place where the external electromagnetic field is low, room is silent and the floor is stable and vibration free. Even interferences in the electrical power network or the existence of any nearby devices can cause severe noise to the lithography process. It is not common to use EBL in the industry because of the low patterning speed. Industry often prefers to replicate the patterns and to have fast and productive process like in EUV stepper rather than having slow patterning which is the case the EBL. EBL is mainly used in R&D in addition to fabricating the master masks for NIL. Additionally, the wafer has to be made from a conductive material or coated with conductive polymer or metal in order to allow a closed loop in the EBL machine circuit.

For this thesis, the column of the electron gun is fixed at a distance of 10 mm from the surface of the sample so that the scanning electron beam can freely scan the desired write field at the appropriate step size. For this thesis, the acceleration voltage is set normally to 10 kV and the aperture value to 10 μm . The alignment is done into two steps. First, the corner of the quarter GaAs sample is locked as origin and the cleaved edge used for aligning the coordinate system and then determining the coordinate system for the sample. The next step is to determine the focal plane of the sample using

three focused points in different locations, usually near the corners of the sample. This is done by several zooming and focusing steps to the features below 100 nm size. In addition, the electron beam is adjusted by removing the stigmation from the beam as well as performing the aperture alignment. Figure 3.9 shows a schematic for the pattern design used in this thesis. The same pattern is repeated in 3 different locations on the wafer in order to compensate for the temperature difference across the sample during the growth inside the MBE reactor. Every location contains 4 different types of pits; single, [011] double, [0-11] double and [010] double pits as shown in the figure. Additionally, the gratings with 2 μm period are added in order to make it easier to locate the pattern areas later.

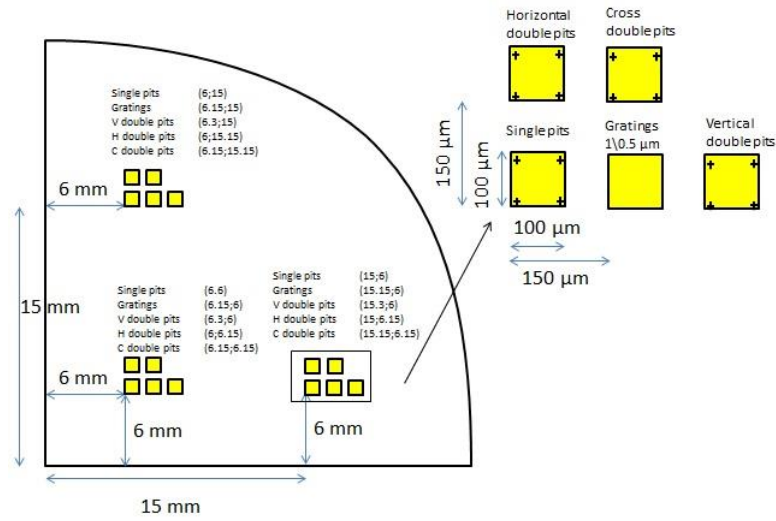


Fig. 3.9: The layout used in thesis. It contains single, horizontal, vertical and cross double pits at 3 different locations on the sample.

The beam current is measured using Faraday cup in order to calculate the correct dose of the electron beam. Using higher EHT means that the electrons are more energetic and thus they will penetrate through the resist with less interaction with the bonds of the PMMA polymer. Additionally, more dose of electron is needed and vice versa in case of having lower EHT voltage. The correct dose must be always tested for the sample with the specific resist thickness, substrate material and electron beam parameters. The write field is selected to be 50 μm x 50 μm which allows the use of 5 nm step size in the patterning. As discussed earlier, one of the main issues with the EBL is the time consuming especially in the patterning. The patterning time depends on the size of the patterned area, the beam current, the dose and the resolution as well.

After the patterning is done, the sample has to be developed immediately in order to remove those cracked bonds by the electron beam. The sample is dipped into the developer which contains MIBK (Methyl isobutyl ketone): IPA with concentration of 3:1 for 30 seconds and then into the IPA for 30 seconds before it is rinsed with water and dried with N_2 .

The GaAs etching step for the EBL and the NIL is almost the same. The GaAs sample is etched by ICP-RIE Plasmalab system manufactured by Oxford instrument shown in figure 3.12. The etching time is 16 seconds. Again the same 20 Watt RF power is used for the RIE which is the power applied between the electrodes. Using more RIE power means higher acceleration for the etching gas radicals. On the same hand, 300Watt is used for the ICP power which controls the current applied to the coils and thus more ICP power leads to more dense plasma by altering the magnetic field in the chamber. Additionally, the pressure is 4.5 mTorr and liquid nitrogen is used to stabilize the temperature during the etching process to 25°C as before in the NIL.

The next step is to remove the PMMA photoresist layer from the sample. Two acetone cups are used. The sample is dipped in each one of them for 3 minutes. The second cup is used in order to make the sample ultra clean after the acetone in the first cup removes most the PMMA from the surface. Immediately after that, the sample is kept in a methanol cup for couple of minutes in order to remove the acetone from the sample surfaces. Finally, it is rinsed with de-ionized water and then blowed with the nitrogen to dry it.

Finally, 10 minutes of 100 Watt RIE oxygen plasma etching at 100 mTorr is applied in order to clean the surface of the sample from any organic residuals. The sample is then ready for the chemical cleaning. The sample is checked with the SEM and AFM in order to check the depth and the diameter of the pits before it is grown in the MBE reactor. The interest to measure the pit size is either to make sure that the process is correct or if it is required to make some changes to the used recipe.

3.1.3. Chemical cleaning

Both the NIL and EBL samples have to be chemically cleaned before loading them inside the MBE reactor. The steps of the chemical cleaning are the same for both samples. The aim of the chemical cleaning process is to remove remaining chemicals used in the process and polymers from the resist for either the NIL or EBL. Furthermore, the mr-UVCur06 used for the NIL process contains inorganic materials which require further cleaning. In addition, there are the gallium and arsenide different oxides which have to be removed from the surface. First, the sample is cleaned with nitrogen and is kept in the IPA for 2 minutes. Furthermore, the sample goes through certain cleaning steps as shown in figure 3.10. The sample is dipped for two minutes into HCl:IPA with concentration of 1:4 before it is rinsed with water and then it is inserted into a composition of $\text{NH}_4\text{OH}:\text{H}_2\text{O}$ with 1:5 concentration for two more minutes. The sample is then rinsed with water and again to the HCl.

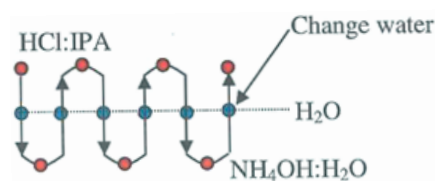


Fig 3.10: The chemical cleaning process steps used in the thesis.

As shown in the figure 3.10, the process cycle is repeated for three times. Moreover, in the last cycle, the water has to be changed in order to keep the sample clean after the water becomes contaminated. Finally, after all the previous steps are done, the sample is kept in the IPA for 2 minutes and then is dried with N_2 . The last IPA step is repeated for two times before the sample becomes ready. The previously mentioned chemical cleaning steps showed the strongest photoluminescence (PL) results [17]. The IPA is mainly used in order to remove the organic impurities. On the other hand, both the HCl and the NH_4OH are used to remove the different oxides [24]. After the chemical cleaning step, [25] has showed that the surface of the sample shall contain arsenide oxide which can be easily removed at low temperature in the oxide desorption process by heating the sample to $590^\circ C$. Thus, the main benefit from the chemical cleaning step is to remove the gallium oxides which can only be removed at very high temperature that the sample cannot withstand. Additionally, the sample must be loaded into the MBE reactor as fast as possible in order to reduce the surface oxidation process in the air which happens immediately after the chemical cleaning step before loading it to the reactor. Figure 3.11 show a summary for the EBL processing steps.

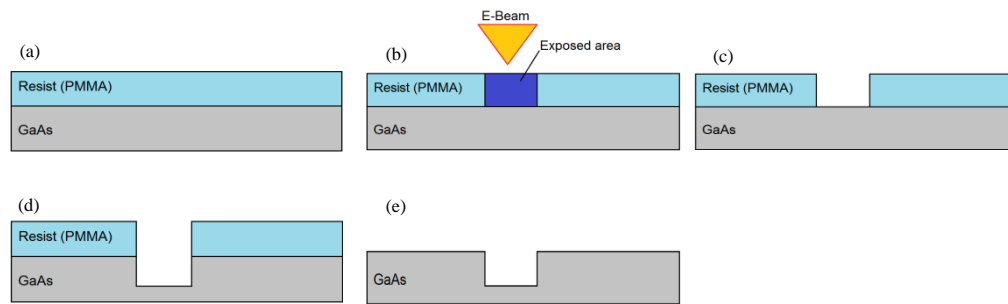


Fig. 3.11: Summary of the EBL process steps (a) applying resist on the surface of the substrate. (b) EBL patterning. (c) Photoresist development. (d) GaAs etching. (e) Resist removal and RIE O_2 plasma cleaning and then chemical cleaning.

3.2. Molecular Beam Epitaxy

MBE was first introduced in 1970s for the purpose of growing pure semiconductor films. However, MBE has had a lot of improvement during the last decades and now it is the mostly used technique for growing epitaxial layer of many different material; metals, semiconductors or even insulators. The operation principle of the MBE is quite simple where atoms are produced by heating up material cells containing different materials. The atoms travel in ultra-high vacuum before they impinge on the hot surface of the wafer. Despite the theoretical easy principle of operation, it took a lot of effort to produce such system with this ultra-high vacuum and precise flow rate control. The MBE is not commonly used in the industry where mass production is needed due to its low yield compared to the other available techniques. However, it is a perfect choice in case it is required to have a precise control over the doping profiles and the growth temperature as well as the growth rate. In the MBE, the quality of the epilayers is better than other epitaxial growth methods. The growth rate is $0.1 - 1 \mu m/h$ [26]. There are

several producing companies like Veeco, Riber and DCA. Figure 3.12 show the schematic construction of the MBE.

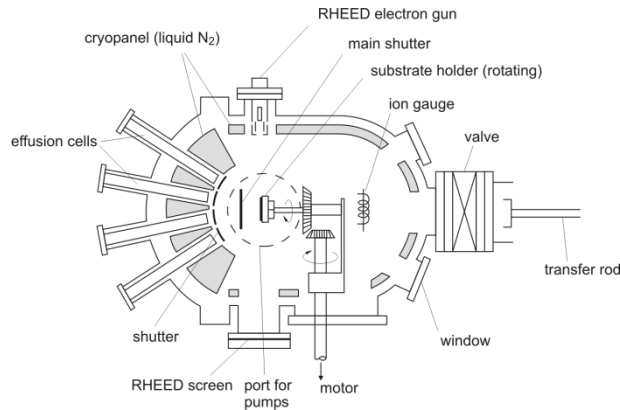


Fig. 3.12 Schematic diagram of the MBE reactor showing its different construction parts [26].

In the schematic, the liquid N₂ cryopanel surrounds the system including the chamber and the sources. It provides the needed isolation between the effusion cells. Additionally, it stops the possible evaporation of any parts other than the material from the cells. The effusion cells have to be designed in a way to provide high stability of the flux in addition to perfectly pure materials. The cells have to be manufactured from material which can resist high temperature (up to 1400°C) for long period. One of the main factors which affect the price of the reactor is the number of the cells. Typically, there are from 6 to 10 cells in the reactor. The stability of the flux has to be closely controlled where it should be more than 99%. In order to achieve that, the temperature has to be controlled with accuracy of 1°C for 1000°C. The effusion cells always end with a shutter in order to control the flux of the cell. The shutter has to operate faster than the flux rate. Additionally, the shutter has to be manufactured from a material that can resist high temperature in order to prevent any possible gas leakage the cell if the one neighbour cell is heated and opened [27].

The manipulator is responsible for the continuous azimuthal rotation (CAR) where it rotates around its axis. This leads to higher uniformity in the same wafer and in the different wafers in case of using multi-wafers reactor. A heater is installed behind the sample to precisely fix the temperature across the whole wafer. The typical pressure inside the MBE is around 10^{-10} Torr which requires involving many different pumps in the reactor like rotary pumps, diffusion pumps, Turbo pump, Ti sublimation pump, ion getter pump and finally a cryo pump [26]. One way to measure the flux is the reflection high energy electron diffraction (RHEED). High energy electron beam (10-50 keV) is directed to the surface of the sample and then is scattered from the first few atomic layers of the surface with a certain angle. The scattered electrons collide with a fluorescent screen showing the surface pattern. Figure 3.13 show the MBE reactor which has been used in the sample growth of both the EBL and the NIL samples as discussed earlier.



Fig. 3.13: The V80 MBE reactor used in the growth of the samples for this thesis.

In order to understand how does the atoms move and grow on each other during the growth, one has to study the growth processes on the surface of the substrate. The growth processes include: 1. adsorption, 2. surface diffusion, 3. desorption, 4. edge diffusion, 5. transformation of ML to bilayer island, 6. dimer formation, 7. dimer decay, 8. step down hopping, and 9. step up jump. Figure 3.14 shows a schematic diagram for the different growth processes which occurs on the surface of the sample [28].

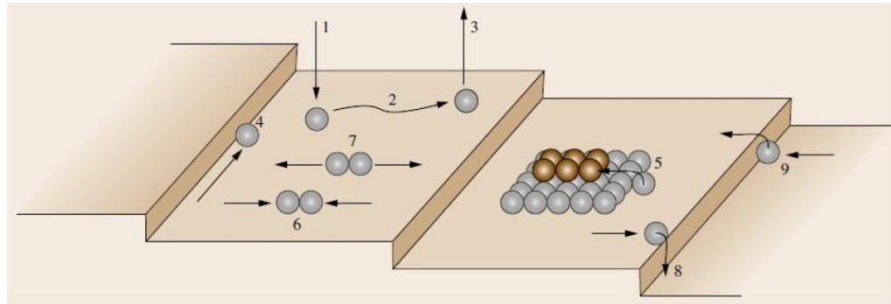


Fig. 3.14: Schematic diagram for the growth processes on the surface of a grown sample inside the MBE [28].

The aim of the next two sections is to discuss about the construction of the sample grown in this thesis. As discussed earlier, two different types of samples are studied in this thesis. First, for the EBL surface samples, the template is prepared when a buffer layer of n-doped GaAs is grown on the wafer of 500 nm with concentration of $2 \times 10^{12} \text{ cm}^{-3}$. The sample is then taken out of the MBE reactor for the processing steps. After the processing steps in the clean room are done as discussed in section 3.1.2 and the sample is chemically cleaned as in 3.1.3, the sample is reloaded to the reactor. It has to be heated to 590°C in order to remove the remaining native oxide. The process of heating to remove the oxide is often called oxide desorption.

Furthermore, one has to grow a regrowth buffer (RGB) layer of intrinsic GaAs for 20 nm layer. The RGB layer has to be grown in order to separate the QD layer and the processed regrowth interface which include many defects. The thickness of the RGB layer is selected upon the best PL results obtained from different samples with different RGB thickness as shown in figure 3.15 [5].

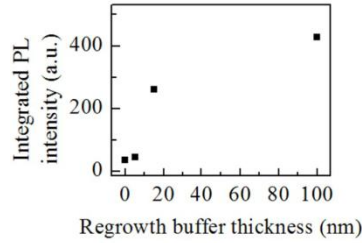


Fig. 3.15: PL intensity (a.u.) as a function of the RGB thickness in (nm) [5].

Finally, there is the QD layer growth in which the indium and arsenic atoms travel from the indium and arsenide cells and are deposited on the substrate surface. The InAs deposition coverage used in the growth is 1.8 ML. Figure 3.16 shows the structure of the sample after the growth.

The sample is measured first with SEM in order to check how the QDs look like and then later with the AFM to measure the height and the shape of the QDs. The surface results from this sample are discussed later in section 4.2.

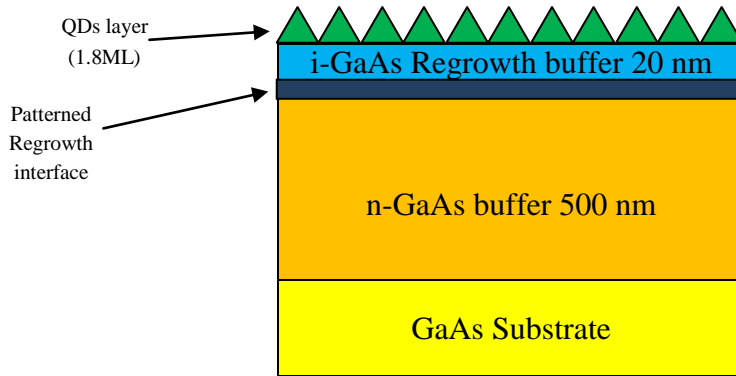


Fig. 3.16: The structure of the EBL surface samples after the growth. The QDs are on top and beneath, there is 20 nm of i-GaAs RGB.

For the NIL samples discussed in section 3.1.1, the same structure is used with minor differences. The RGB layer size is increased to 30 nm due to the difference in the patterning technique – instead of EBL – which leads to different defects. Additionally, there is the Schottky diode on top and an ohmic contact on the back. The Schottky contact contains 500 nm silicon n-doped GaAs layer with a concentration of $2 \times 10^{16} \text{ cm}^{-3}$. Upon the semiconductor layer, there is a 100 nm chromium layer which is grown by using E-beam evaporation. Together the metal and the semiconductor layers work as a Schottky contact. On the other hand, the indium droplet together with GaAs substrate

forms the ohmic back contact. For this sample, the C-V measurements are discussed in order to realize how those curves will change due to the site-controlled QDs layer and the patterning process.

Figure 3.17 shows the full structure of the Schottky diode samples. However, in the studied samples, it is not necessary that all the samples shall include the QD layer. Some samples are studied after only having regrowth interface without including any patterns and RGB. Thus, it is possible to observe the effect of each step separately on the electrical properties of the Schottky diode.

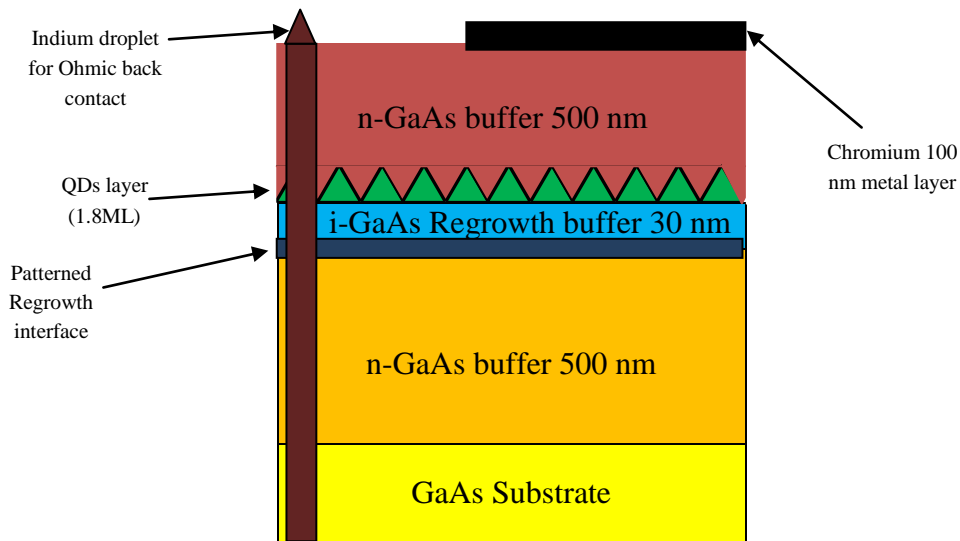


Fig. 3.17: The optimum structure for the NIL patterned samples with site-controlled QDs layer. On top, there is a metal semiconductor layers which work as a Schottky diode.

3.3. Characterisation

The aim of this section is to show the principle of operation needed in order to characterize and measure the structural and electrical properties of the samples involved in this thesis. First, for the surface EBL processed samples, it was required to check the nature of the single and the double QDs. The study also includes different spacing between the double QDs. For the surface characterization, there have been two options used in this thesis SEM and AFM.

On the other hand, the electrical characterization of the Schottky diode samples – which have been processed by NIL – is presented in the C-V measurements of the diode with the embedded QD layer inside.

3.3.1. Scanning Electron Microscopy

The SEM was first introduced in 1950's and since that it is being used widely in different fields. It has many advantages over the ordinary microscope. It is a high resolution

microscope in which it can show details down to a couple of nanometers. Additionally, it has a good depth of field which give an advantage to focus larger area on the same image. However, the SEM is operated only on vacuum in the order of 10^{-6} Torr, thus samples which are not stable at low pressure, are not suitable for ordinary SEM but variable pressure systems can expand this pressure range. Additionally, usually conductive samples can be imaged in order to allow the electrons to be earthed through the sample; otherwise a layer of metal (conducting material) has to be inserted above or below the sample [29].

Figure 3.18 shows the schematic diagram of the SEM system. The basic principle in the SEM depends on an electron gun which is the source of electrons. The electrons are accelerated and directed to sample. The electron beam is focused by controlling the diameter of the beam reaching the sample using the condenser and the objective lenses. The electron beam is controlled precisely by using a series of microscale openings which are called the apertures. The stage which holds the sample can be raised, lowered and tilted for better imaging. When the electron beam hits the sample surface, backscattered and secondary electrons in addition to X-rays are ejected from the sample. The X-rays and the ejected electrons are detected and converted into an electrical signal. The signal is processed using high technology image processing system to generate the image [30].

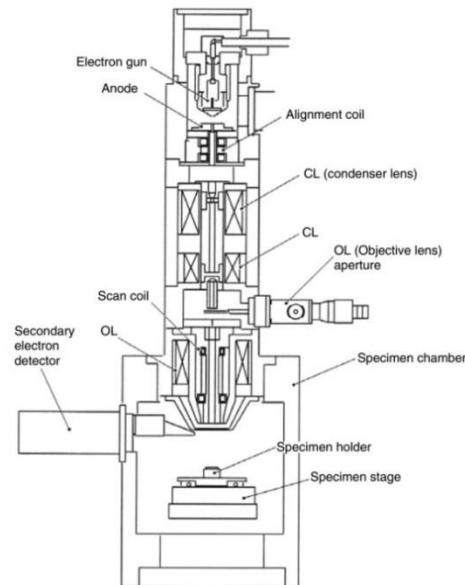


Fig. 3.18: SEM schematic diagram showing different parts inside the machine [30].

As mentioned earlier, the SEM has been used in our project in order to image and to study the pits and QDs structure for different samples. In our project, after the InAs QDs layer is grown on the GaAs substrate in the MBE, the sample is brought back to the clean room for study. The sample is loaded into the SEM. There is no need to use high EHT value in order not to charge the sample under measurements. It was often enough to use 2 kV with $10\ \mu\text{m}$. The rest is to zoom and focus several times until one

can image the QDs in interest. The same machine shown in figure 3.8 used in the EBL is used for imaging.

3.3.2. Atomic Force Microscopy

Scanning group microscopy refers to a group of imaging techniques which collect images of the sample surface by moving a probe over that surface in a raster pattern. As the probe moves, it scans the height of the surface. AFM is the most common scanning microscopy technique.

All scanning probe techniques have a small probe, a feedback method and a fine control of the distance between the tip and the sample surface. Various methods can be used to send the signal to the feedback. The feedback control assesses the distance between the tip and the sample surface. If the distance between them is small, the feedback loop signal, by the control on a piezo crystal, lowers the sample holder by contracting the piezo crystal. On the other hand, if the distance is too large, the piezo crystal is stretched in order to move the sample closer to the tip. The image is formed by plotting the horizontal and vertical scanning on the surface of the sample.

AFM uses a silicon nitride tip connected on the end to a silicon cantilever spring. The feedback signal is based on the change of the force between the tip and the sample which changes the angle of the cantilever and moves the spring. A laser beam is reflected back from the back of the tip depending on the height of the scanned area. Figure 3.19 shows a schematic diagram of the AFM theory.

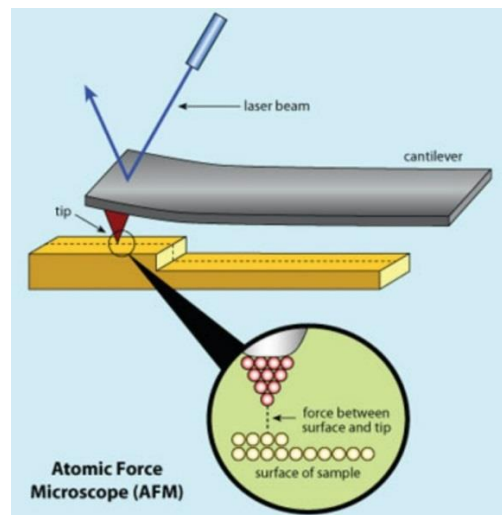


Fig. 3.19: Schematic diagram showing the AFM working principle.

In the AFM, there are three scanning modes; contact mode, non-contact mode and tapping mode. For the samples scanned in this project, only tapping mode was used. In the tapping mode, as the name implies, the tip gently oscillates as the sample is being scanned. The amplitude oscillation is used as the feedback signal. The tapping mode is

used in order not to destroy the QD as in the case if the contact mode is used in which the tip is all the time in contact to the surface of the sample. Figure 3.20 show the AFM machine which is used in this project. On the same hand, the results chapter shows the study of the scanned Quantum double dot (QDD) with different spacing. The machine is manufactured by Veeco metrology group and the model of the machine is Dimension 3100.

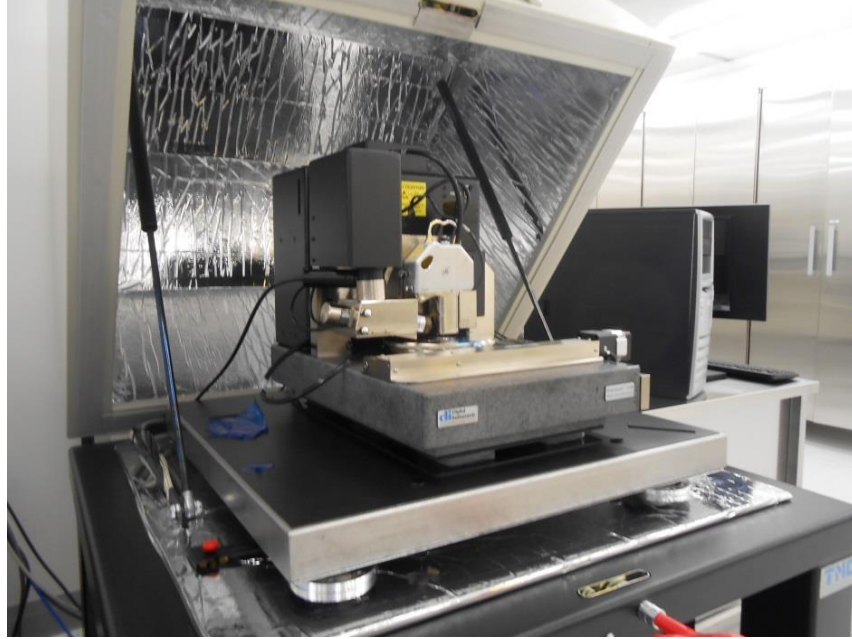


Fig.3.20: Veeco AFM machine used for imaging the site-controlled QDs samples in the project at the ORC clean rooms.

3.3.3. Capacitance voltage measurements in semiconductors

The capacitance of the depletion region depends on the depletion region width W as discussed earlier in section 2.3. Additionally, it depends on the doping level in the semiconductor as well. Thus, the C-V measurements can be used to calculate the depth profile of the carrier concentration.

According to the depletion layer approximation, the charge fluctuations happen only at the edge of the depletion layer. Thus, with this approximation, it is possible to deduce the doping profile for any doped semiconductor [13]. The doping density level $n(w)$ is calculated from the slope of the C-V plot diagram and can be calculated from equations (2-2) and (2-3) as:

$$n(w) = \frac{2}{A^2 q \epsilon_o \epsilon_s \left[\frac{d(1/c^2)}{dV} \right]} \quad (3-1)$$

Thus, the depth profile can be obtained from equation (3-1) with the aid of equation (2-2) and (2-3) in which [13]:

$$\frac{1}{C^2} = \frac{2(V_o - V_b)}{A^2 q \epsilon_o \epsilon_s N_d} \quad (3-2)$$

3.4. Schottky diode behaviour with Quantum dot layer

When a QD layer is inserted into a Schottky diode as shown in figure 3.18, the charge carriers inside those QDs can be understood as a 2-dimensional homogenously distributed electric charge density. The negative charge density due to the filled electron states in those QDs ρ_{QD} is written as:

$$\rho_{QD} = -qn_{QD} = iqN_{QD}, \quad (3-3)$$

where the n_{QD} is the electron density in the QD layer and N_{QD} is the (area) density of the QDs. The i refers to the electron occupation in the QD states. For example, if $i=2$, then it means that s-states are fully occupied. It can be assumed that the i value is constant for all QDs in such layer.

If assumed that the QD layer is placed in a distance of x_{QD} from the Schottky contact then the potential $V(x)$ for the whole structure can be derived as [31]:

$$V(x) = \frac{qN_d}{2\epsilon_o\epsilon_s}(w-x)^2 - \begin{cases} 0 & x_{QD} \leq x \leq w \\ \frac{qn_{QD}}{\epsilon_o\epsilon_s}(x_{QD}-x) & x \leq x_{QD} \end{cases} \quad (3-4)$$

From the equation shown above, the potential $V(x)$ depends on the depletion width. Thus, the potential depends on the applied voltage as well. The maximum value of the potential rises at $x = 0$ at the edge of the Schottky contact. The potential should be equal to the total band bending which is equal to the $V_o - V_b$.

$$V(x = 0) = V_o - V_b = \frac{qN_d}{2\epsilon_o\epsilon_s}w^2 - \frac{qn_{QD}}{\epsilon_o\epsilon_s}x_{QD} \quad (3-5)$$

The equation (3-5) consists of two parts; the first term is caused by the ionized donors in the depletion region of the n-GaAs at the edge of the Schottky contact ($x=0$). The second term explains the accumulation of the charges in the QDs and how it will have a remarkable effect on the overall potential. The depletion width can be obtained from the equation (3-5); one shall get [13]:

$$w = \sqrt{\frac{2(\epsilon_o \epsilon_s (V_o - V_b) + q n_{QD} x_{QD})}{q N_d}} \quad (3-6)$$

Now by substituting in equation (2-2), one can easily obtain the depletion capacitance as:

$$C = \epsilon_o \epsilon_s A \sqrt{\frac{q N_d}{(\epsilon_o \epsilon_s (V_o - V_b) + q n_{QD} x_{QD})}}, \quad (3-7)$$

It is possible to assume that $N_d \gg n_{QD}$, the assumption is quite logical especially in case of high doping concentration, thus equation (3-7) can be written as:

$$C = \epsilon_o \epsilon_s A \sqrt{\frac{q N_d}{2 \epsilon_o \epsilon_s (V_o - V_b)}} \cdot \left[1 - \frac{q n_{QD} x_{QD}}{2 \epsilon_o \epsilon_s (V_o - V_b)} \right] \quad (3-8)$$

The first term shows the same capacitance formula shown earlier. Thus, it is the capacitance at equilibrium where $t = \infty$ where the time is enough that the electrons have escaped from the confined energy states. One can call this equilibrium part as C_∞ where [13]:

$$C_\infty = \epsilon_o \epsilon_s A \sqrt{\frac{q N_d}{2 \epsilon_o \epsilon_s (V_o - V_b)}} \quad (3-9)$$

At certain bias voltage, there will be no electron trapped in the QDs layer, the deselection region width can be called as w_∞ which occurs at $n_{QD} = 0$. Now by substituting in (3-6), one shall get $q N_d w_\infty^2 = 2(\epsilon_o \epsilon_s (V_o - V_b))$ and then by substituting back in (3-8):

$$C = C_\infty \cdot \left[1 - \frac{n_{QD} x_{QD}}{w_\infty^2 N_d} \right] \quad (3-10)$$

The existence of occupied QDs leads to local bending in the conduction band due to the coulomb charging of the QDs. Figure 3.21 shows the conduction band and its relative charge density for both a charged and uncharged QDs case.

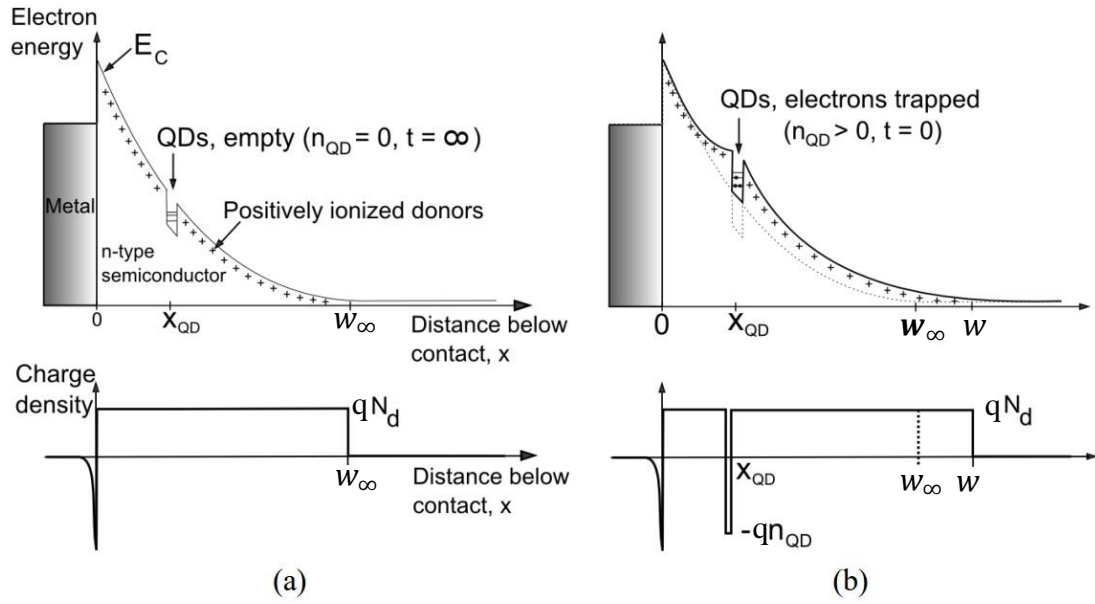


Fig. 3.21: Schematic diagram showing the conduction band bending as well as the charge density in the depletion region of for a Schottky diode have an (a) uncharged and (b) charged QDs layer [31].

The next part of this section discusses about the C-V profiling for a Schottky diode with QDs layer structure. One should expect similar behaviour to the one seen for a Quantum well (QW) structure [32].

When the bias voltage on the Schottky diode varies, the Fermi level E_F is changed relatively. When the Fermi level moves through the QD level, the differential capacitance shall be influenced. It is important to choose the frequency and the temperature which allow the thermal equilibrium [33]. Figure 3.22 shows the C-V profiling of such Schottky structure with the QD layer embedded inside. The dashed line in the lower diagram shows the typical C-V plot in case of bulk material. Now, duo to such quantum state at the depth of x_A whose energy level is E_A , there is a constant capacitance region in which the capacitance does not change with the change of the bias voltage.

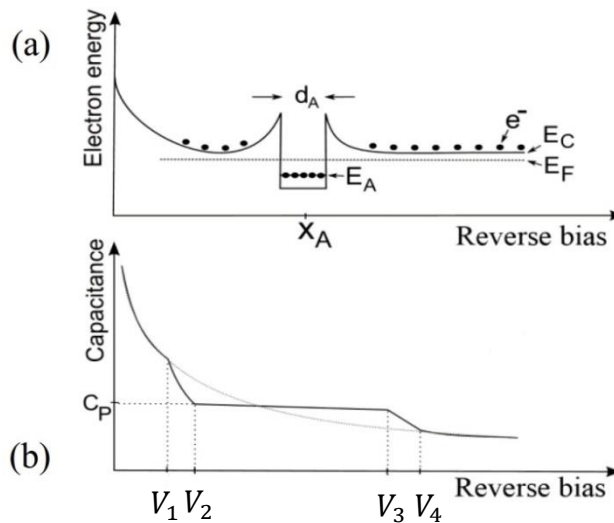


Fig. 3.22: C-V measurements for a heterostructure with QD layer embedded inside. (a) The band bending of the structure. (b) The C-V plot for the heterostructure.

The capacitance variation through the structure can be divided into 5 parts as follow;

- 1- $V < V_1$, the bias voltage is not enough to make the depletion region reach the QD layer. The capacitance behaviour is the same as for the normal bulk structure.
- 2- $V_1 < V < V_2$, a decrease in the capacitance occurs where the depletion region above the QD adds to the depletion region which takes place due to the band bending.
- 3- $V_2 < V < V_3$, the capacitance remains constant due to the screening caused by the large amount of carriers located in the QW.
- 4- $V_3 < V < V_4$, the QD is empty; the depletion region beneath the QD starts to add to the total depletion region. Thus, the capacitance decreases again.
- 5- $V_4 < V$, the depletion region has passed the QD layer. The capacitance changes normally again like in bulk semiconductors.

4. RESULTS

The aim of this chapter is to present the experimental results done as a part of the PhotonicQCA project. The results include the sample statistics which were done mainly to find out the suitable diameter for the pits to cover the needs of the project. From that, there is the study of the spacing between the QDD. In the study, it is shown how it was possible to grow QDD with different spacing and in different orientations. The later part explains the electrical characterization of a Schottky diode samples with QD layer embedded inside. The C-V curves are shown after each step in order to discover the effect of each step during the sample preparation.

4.1. Sample Statistics

In this section, a study has been done in order to deduce what could be the most suitable pit size in which the site-controlled QDs are grown inside. In the study, the occupational probability for single, [011] and [0-11] orientations are studied for 100 samples. The [010] orientation is not discussed in this section however it will be discussed later in section 4.2.3. The [011] orientation is called horizontal double pits (HDP), [0-11] is called vertical double pits (VDP). Finally, the [010] orientation is called cross double pits (CDP). The aim was to find out the best diameter to allow the highest occupation probability of a single QD inside each pit. Figure 4.1 shows the probability of QDs to occupy single pits. The study included 30, 40, 50 and 60 nm pits.

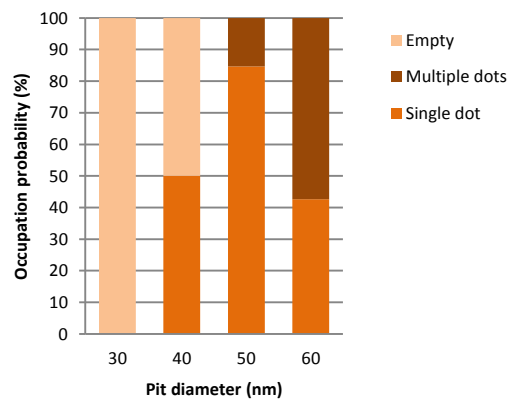


Fig. 4.1: Occupation probability of single pits with different diameters.

The 30 nm pit size has been always empty. The 40 nm pit size showed 50% empty pits and the other 50% was occupied with single QD. For 50 nm, about 85% of the pits were filled with single QD. Only 15% were filled with multiple QDs. Finally, for the 60 nm

study, over 65% were actually occupied with multiple QDs while only 45% were filled with one QD.

For the HDP, figure 4.2 shows the occupation probability with respect to the diameter of the pits.

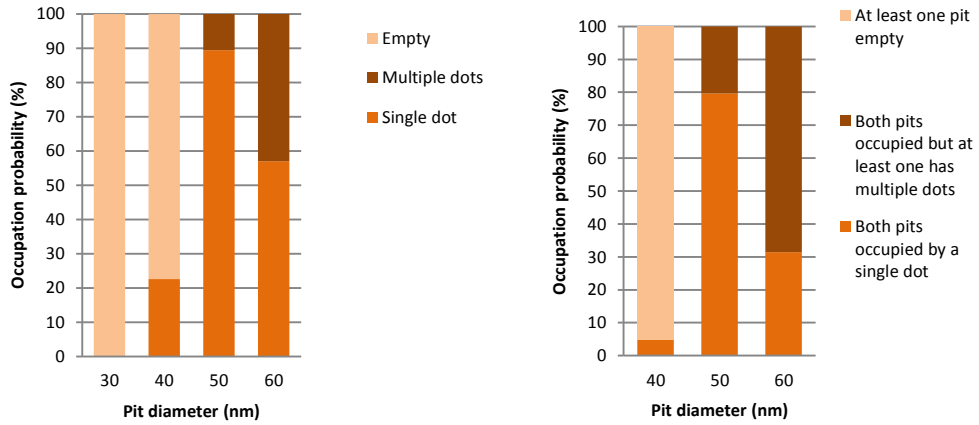


Fig. 4.2: Occupation probability study for the HDP. The study includes 30, 40, 50 and 60 nm diameter pits.

The study of the HDP shows that for 30 nm diameter pits, the pits were all empty. For 40 nm case, only 25% of the pits were occupied, however, at least 95% of the HDP had one pit of them to be empty. The study of the 50 nm pits showed that about 90% of the HDP were filled with a single QD. On the same hand, around 80% of both of them were filled by only single QD and only 20% were occupied by multiple QDs. Furthermore, for the 60 nm diameter pit samples, the percentage of the occupied HDP with only single QD is decreased to 57% from 90% as it was in the 50 nm case. Only 32% of the HDP were occupied by single QD each.

Finally, for the VDP, the study which is similar to the HDP is shown in figure 4.3.

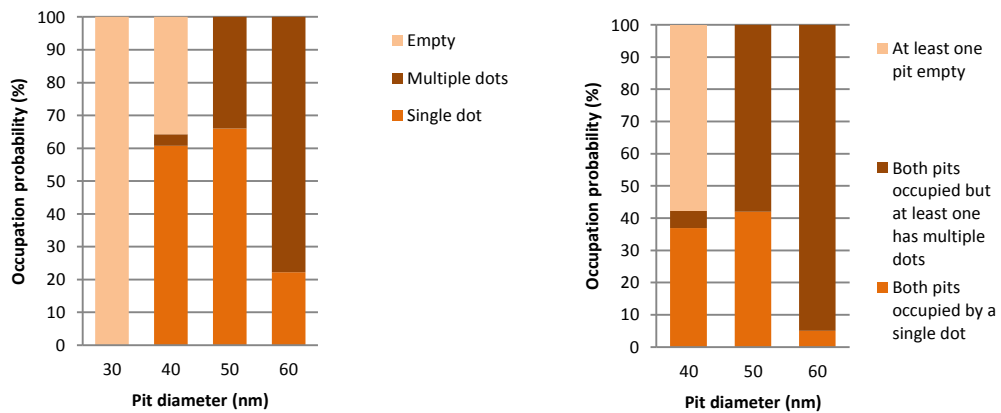


Fig. 4.3: Occupation probability for the VDP. The study also includes 30, 40, 50 and 60 nm diameter pits.

Similar to the HDP, the 30 nm diameter pits were not occupied at all. For 40 nm, around 60% of the pits were filled with single QDs. 5% of the pits were filled with multiple QDs. About 35% of the pits were left empty. Additionally, 55% of the two pits had one pit to be empty while only 5% had both of the pits to be filled. The study of the 50 nm diameter samples showed that 65% of the pits had single dots and 45% of those filled pits had only single QD per pit. While 55% of the double pits were occupied in a way that at least one pit had multiple QDs. In case of the 60 nm pits, about 75% of the pits were occupied but with multiple QDs. Furthermore, for every double pit, it is found that 95% had at least one pit of them to be filled by multiple QDs and only 5% showed that both of the pits were occupied by single QD per pit.

According to this study, 50 nm diameter pits resemble the most suitable diameter for the project. They show the highest occupation probability over 30 and 40 nm pits. Furthermore, they have better results in which each pit is occupied with single QD instead of multiple QDs which is the case of 60 nm pits. Due to this finding, only 50 nm diameter double pits were used but with different spacings and orientations as it will be shown in the next section.

4.2. Double QDs with 50 nm pit wide

As discussed in the previous section, the 50 nm pit is found to be interesting fulfilling the requirements for the PhotonicQCA project. In this section, AFM results for both empty and filled pits are shown in three different polarizations; HDP, VDP and CDP. The pits are studied with different spacing before it is grown and again measured with AFM in order to compare the theoretical and measured results. All the experimental images are shown in the appendix 1.

4.2.1. [011] double pits

Figure 4.4 shows the study for the HDP [011]. After the lithography and the etching process are done, the sample is measured with AFM where it shows that the two pits are merged together for the spacing's: 45, 50, 55 and 60 nm. At around 65 nm, the distance of the pits starts to be clearly separated. The distance between the pits increases then gradually with the increase of the distance. There are many factors limiting the minimum spacing between the pits, for example: the quality of the photoresist, the level of anisotropic etching. As shown in the figure, there is about 10 nm extra distance between the two pits relative to the theoretical assumption.

After the sample is grown, the spacing between the QDs is studied again to check how the QDs shall fill the empty dot with various spacings. Figure 4.5 shows the comparison between the theoretical and measured spacing between the QDs with different spacing. Unlike the empty HDP, the spacing between each two horizontal QDs increases steadily with the increase of the supposed spacing.

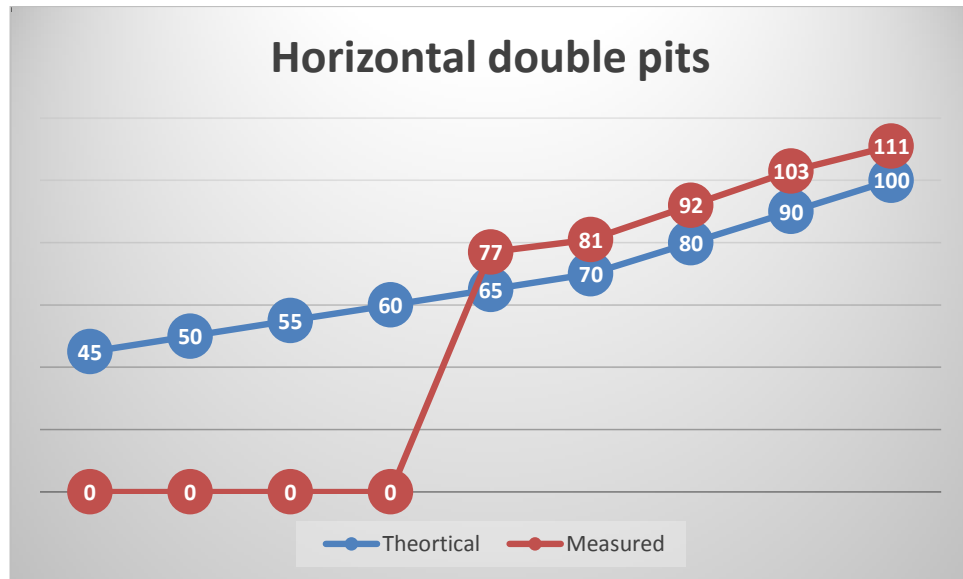


Fig. 4.4: Comparison between the theoretical (supposed by lithography) and practical HDP includes 10 different spacing's from 45 to 100 nm.

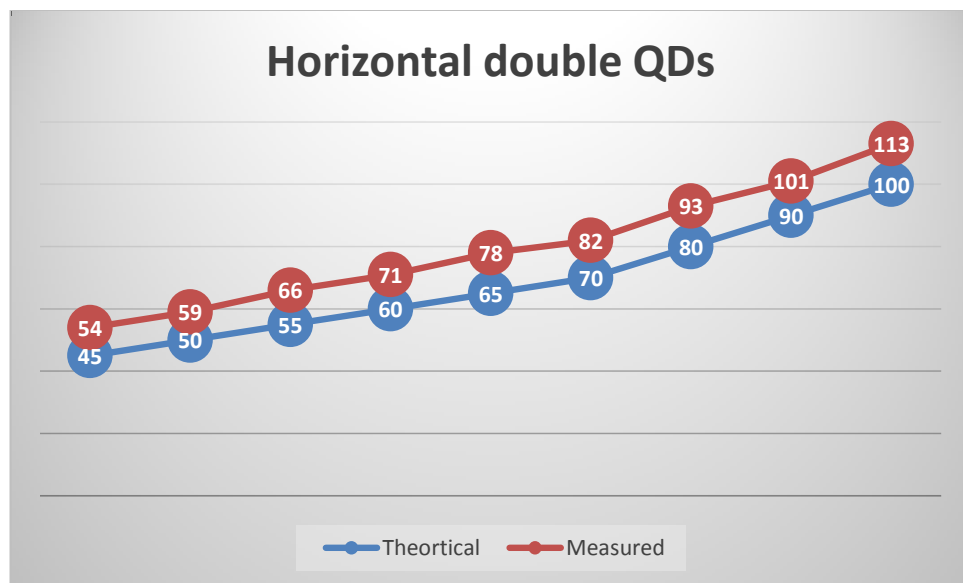


Fig. 4.5: Comparison between the theoretical and practical two horizontal QDs (filled pits).

4.2.2. [0-11] double pits

As shown in figure 4.6, the VDP seems to be merged like the HDP case. However, the main remarkable difference arises in the increased measured spacing than the theoretical one. The minimum spacing which can be obtained by the VDP is 85 nm.

Additionally, as long as the spacing between the two QDs is less than 70 nm, the QDs are merged into one QD only. They are only separated when the spacing between them

goes above 70 nm. The measured spacing between the QDs shows more than 20 nm of extra spacing from the theoretical spacing.

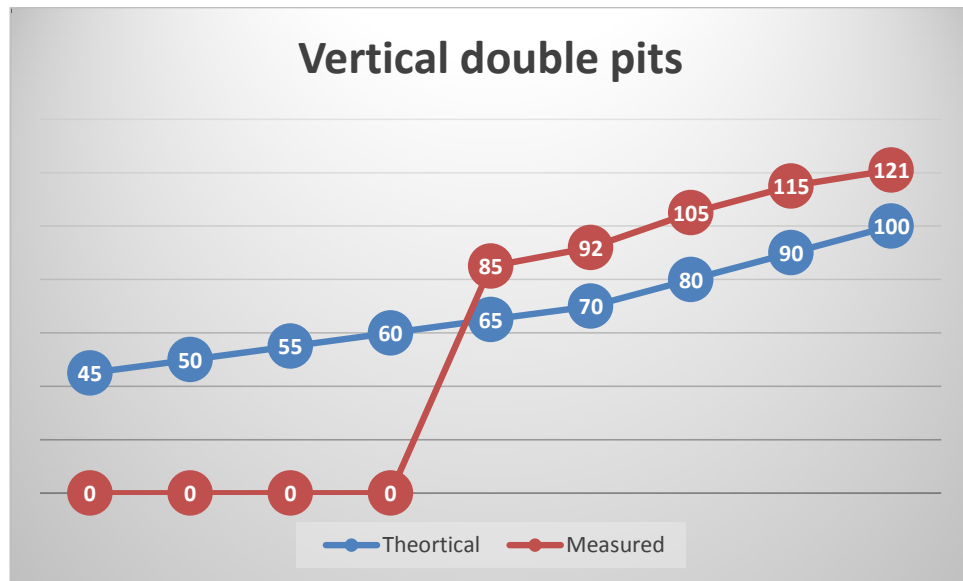


Fig. 4.6: Comparison between the theoretical and practical VDP.

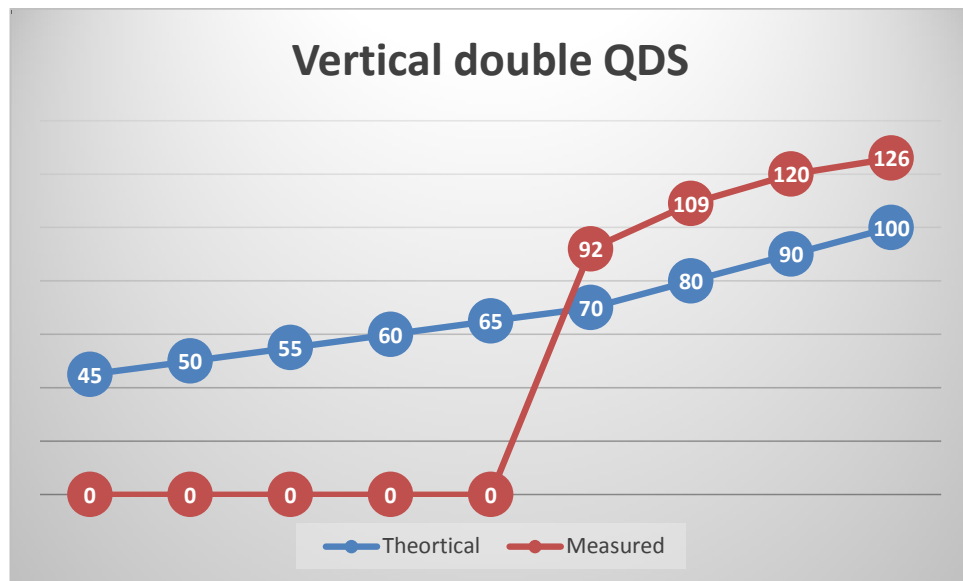


Fig. 4.7: Comparison between the theoretical and practical two vertical QDs.

4.2.3. [010] double pits

Finally, for the CDP, as shown in figure 4.8, the two etched CDP seemed to be one big pit until the distance between them is 106 nm. In other words, the measured spacing is increased by 45 nm from the intended one.

On the other hand, the cross double QDs are also interesting in a way that reasonably low spacing can be obtained. The minimum obtained spacing is found to be about 70 nm. The spacing between the two QDs increases rapidly with the increase of the spacing between them.

It is also good to mention that the orientation for the cross double QDs remain horizontal until the spacing between them is around 70 nm then it starts to have the cross direction instead. The images presented in appendix I show clearly the change of the orientation from horizontal to cross as mentioned earlier.

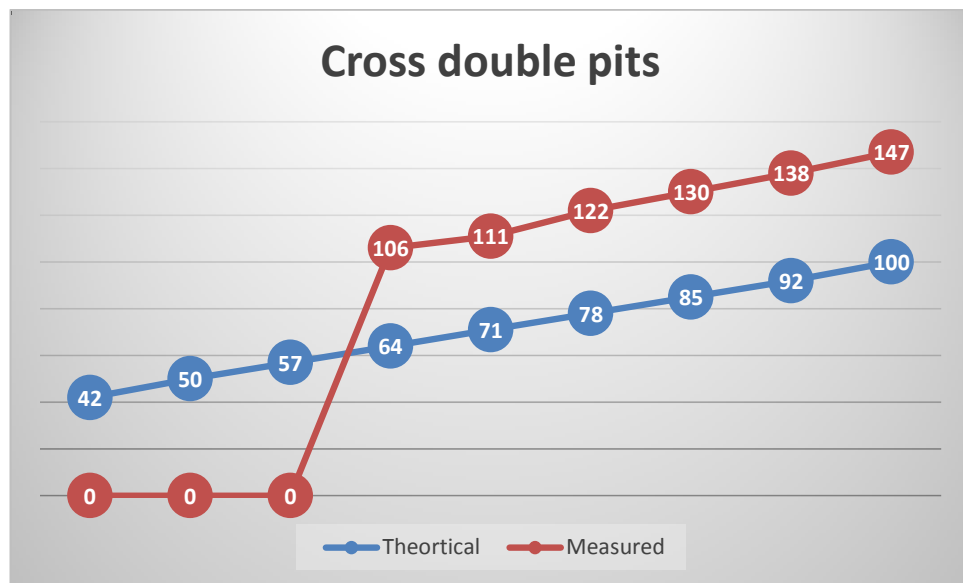


Fig. 4.7: Comparison between the theoretical and practical CDP.

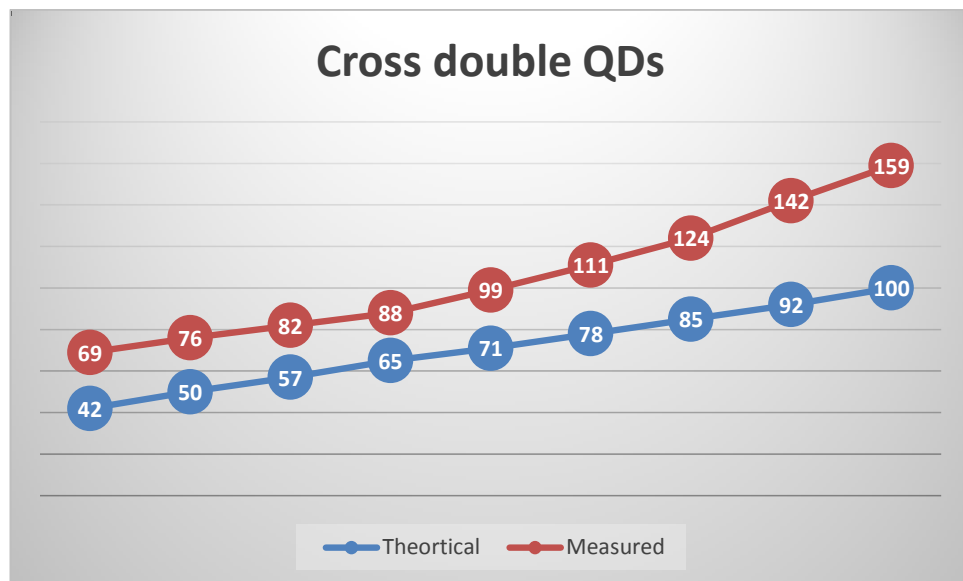


Fig. 4.8: Comparison between the theoretical and practical two cross QDs.

4.3. Electrical characterization for Schottky diode structure with embedded Quantum dots layer

The aim of the section is to present the C-V measurements for the Schottky diode structure with the embedded QDs layer. 9 samples have been used in order to deliver the study shown in this thesis. The samples had to go through many steps of processing and growth before measurements; growing the buffer layer (n-GaAs) of 500 nm for all samples, NIL process, etching the sample, chemical cleaning, then taking the sample to the MBE while it goes through the oxides desorption step, RGB growth and finally the QDs growth. At the end, the samples have the evaporation of both a Schottky and an ohmic back contact on top and to the bottom relatively. Table 4.1 shows the different samples used in the study. As shown in the table, it is not necessary that all the samples have gone through all the process steps. The C-V measurements at different temperature and a discussion for each sample are presented after the table.

Process steps Samples name	NIL process	Chemical cleaning	Oxides desorption	RGB growth	QDs growth
ASN-3467					X
ASN-3466			x	x	X
ASN-3462			x	x	X
ASN-3461		X	X	x	
ASN-3460		x	X	x	X
ASN-3465	x	x	X	x	
ASN-3465*	x	x	X	x	
ASN-3464	x	x	X	x	X
ASN-3464*	x	x	X	x	X

Table 4.1: Summary includes the different samples used in this thesis. The table includes the different process steps used in each sample.

The ASN-3457 is a reference sample in which only self-assembled QDs are grown instead of site-controlled QDs. Thus, there were no need for any processing steps (i.e.: NIL, chemical cleaning, oxides desorption or RGB growth). Figure 4.10 shows the C-V measurements of the sample at different temperatures.

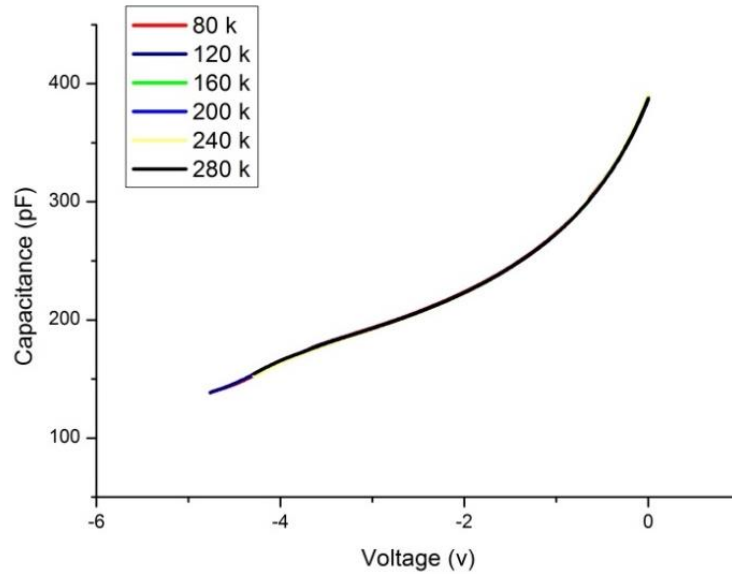


Fig. 4.10: C-V curves for the reference sample ASN-3467 at different temperature.

The capacitance curve remains the same at all temperature as shown in the graph. The capacitance change with respect to the reverse bias voltage looks ideal.

For the ASN-3466, after the buffer layer of 500 nm is grown on the substrate, the sample is taken out of the reactor and is inserted back. The sample has to be heated to 610°C for 10 minutes in order to remove the created regrowth interfaces. Figure 4.11 shows the C-V curve of the sample at different temperatures.

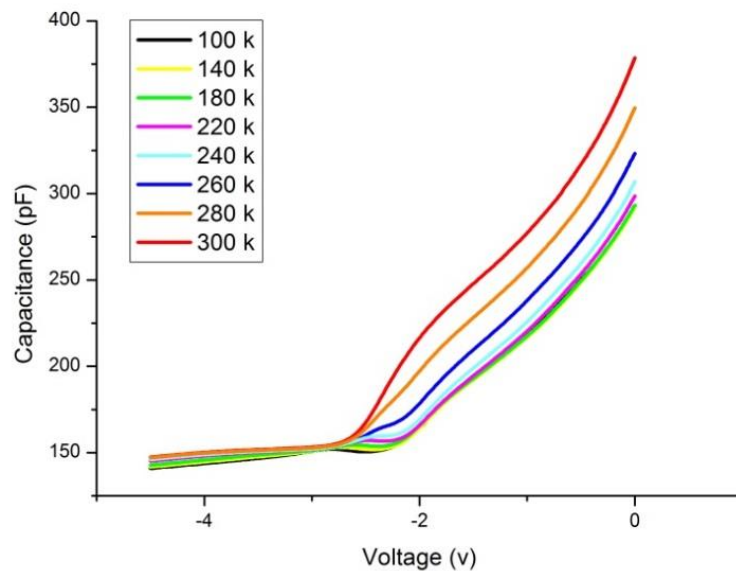


Fig. 4.11: C-V curves for ASN-3466 at different temperature. The sample is only taken out and then inserted back to the reactor before having the oxide desorption step at 610 °C for 10 minutes.

As shown in the graph, the capacitance does not change with the bias voltage until a certain point at which the depletion region pass over the defects layer due to the regrowth interface. The higher temperature showed higher capacitance than lower tem-

perature capacitance due to having more thermally excited charges to contribute to the overall capacitance.

The main difference between the ASN-3462 and the previous sample (ASN-3466) is only the oxide desorption step. The oxide desorption step made for the ASN-3462 is more suitable for NIL samples. The temperature is only raised to 590°C for 5 minutes. The temperature is decreased in order to give more stability for the site-controlled QDs to be grown in the pits. In [5], it is shown that samples grown with higher temperature oxide desorption step had lower occupation probability than lower temperature samples. Figure 4.12 shows the C-V curve of ASN-3462 which has only one difference with ASN-3466, modifying the oxide desorption step.

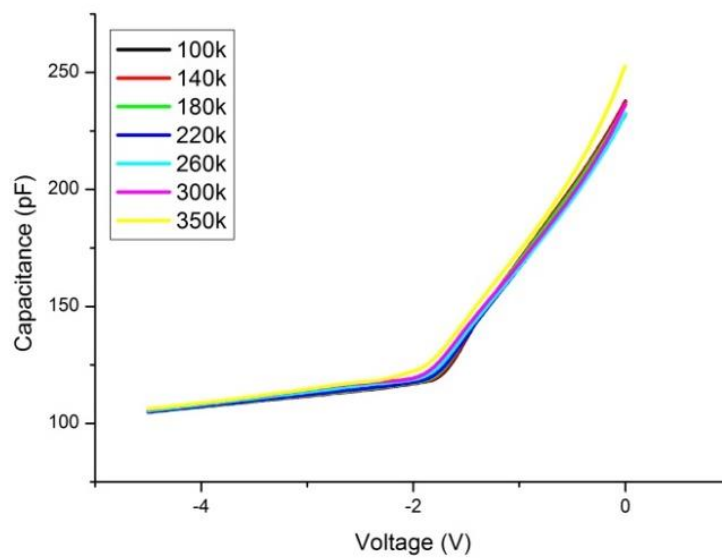


Fig. 4.12: C-V curve for ASN-3462 sample. Similar to ASN-3466 with modified oxide desorption step.

It is noticed that the magnitude of the capacitance all over the curve is decreased. Additionally, the capacitance is kept constant with bias voltage increase due to the regrowth interfaces.

The rest of the samples discussed in this study have one common step which is the chemical cleaning. As discussed earlier in the process chapter. The chemical cleaning step is mandatory for all the processed samples before they are loaded to the reactor, otherwise the remaining resist materials and the oxide will lead to an increase in the pressure during the growth which will cause the reactor to shut down and growth failure.

ASN-3461 includes only the chemical cleaning step without any NIL process. In other words, after the n-GaAs buffer layer is grown, the sample is taken out in order to be chemically cleaned and then is loaded back to the reactor and is heated as usual to remove the oxides layer before the RGB is grown. The capacitance of the sample is remarkably degraded as shown in figure 4.13.

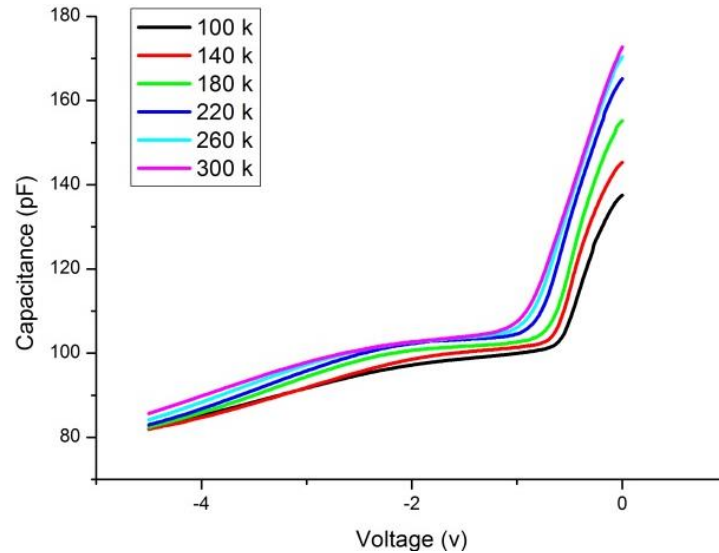


Fig. 4.13: C-V curves for ASN-3461 at different temperature. It is shown the degradation of capacitance all over the curve due to the chemical cleaning step.

The capacitance remains almost constant up to -1 V reverse bias. The highest recorded is capacitance is 180 pF which is down from about 400 pF in the reference sample (ASN-3467). Thus, the overall capacitance is also decreased.

The only addition made to ASN-3460 was to grow a self-assembled QDs layer on top of the RGB since there was no NIL process involved in the process. Figure 4.14 shows the C-V measurements for the ASN-3460 sample. It is noticed that the defects due to the chemical cleaning step are still screening the depletion region to change with the reverse bias increase. As shown, the capacitance is constant up to almost -1 V. The magnitude of the capacitance all over the curve is still remarkably below the reference sample. It is noticed that the overall capacitance increases by the rise of temperature. The electrons are thermally excited and thus the electrons are easily removed from the chemical cleaning defects and shall contribute to the overall capacitance.

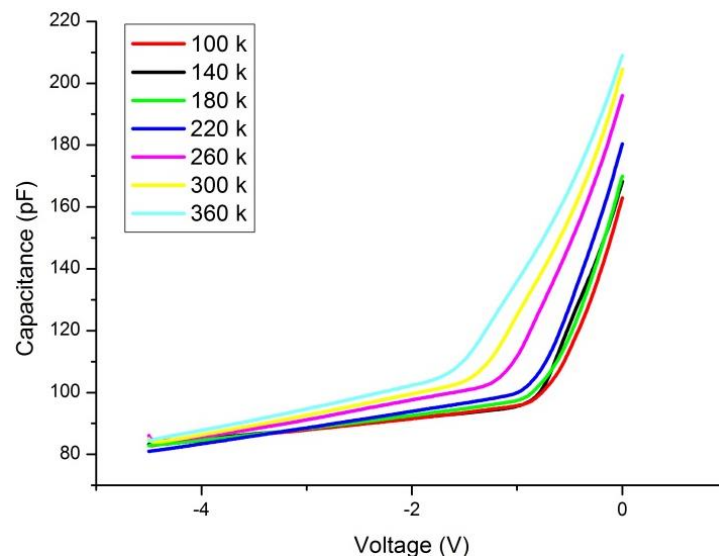


Fig. 4.14: C-V curve for ASN-3460 at different temperature. The only addition from ASN-3461 is growing the self-assembled QDs layer.

In ASN-3465, the sample is processed by the NIL. Furthermore, one had to chemically clean the sample before it is loaded to the MBE reactor. As shown in figure 4.15, the sample has the same behaviour due to the chemical cleaning step.

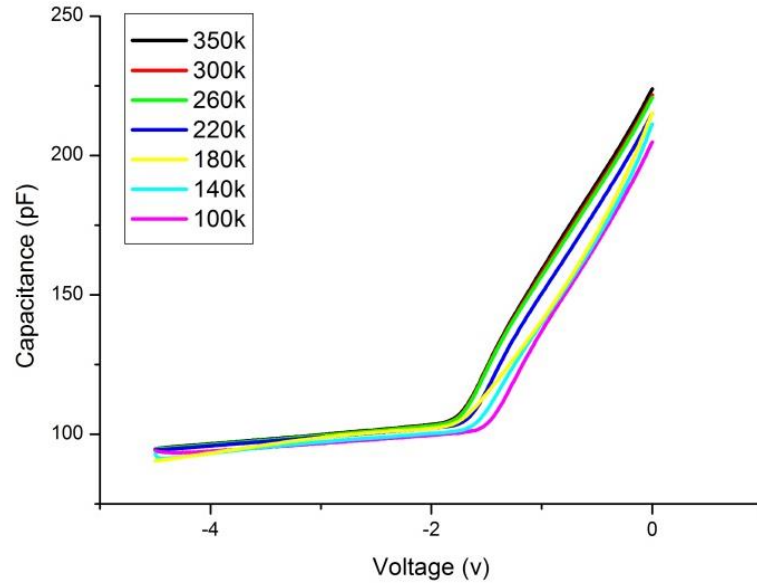


Fig. 4.15: C-V measurements for ASN3465. NIL process is done to the sample and is chemically cleaned and is loaded to the reactor. The capacitance behavior is similar to previous samples.

The difference between ASN3465* and ASN-3465 is only that the part of the sample under measurements is different. For ASN-3465*, C-V measurements is carried out for the unpatterned area instead of the patterned NIL area like in ASN-3465. Figure 4.16 shows the C-V curve for ASN-3465* at different temperature.

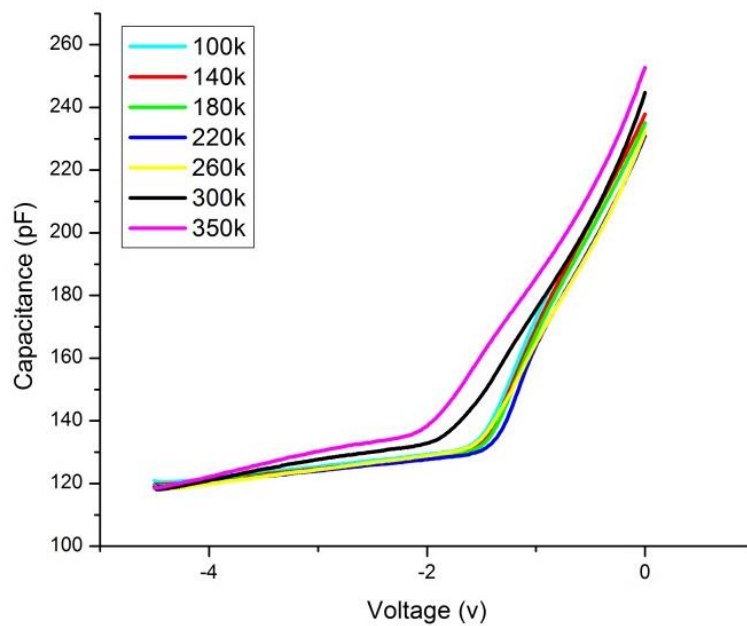


Fig. 4.15: C-V curve for ASN-3465* at different temperature. The part of the sample under measurements is outside the patterned area unlike ASN-3465.

Finally, for ASN-3464 and ASN-3464*, both are grown to have site-controlled QDs layer on top of the RGB layer. Again, ASN-3464* sample results are based on measurements done on the unpatterned area unlike the case in ASN-3464*. Figure 4.16 and 4.17 show the C-V measurements for ASN-3464 and ASN-3464* respectively.

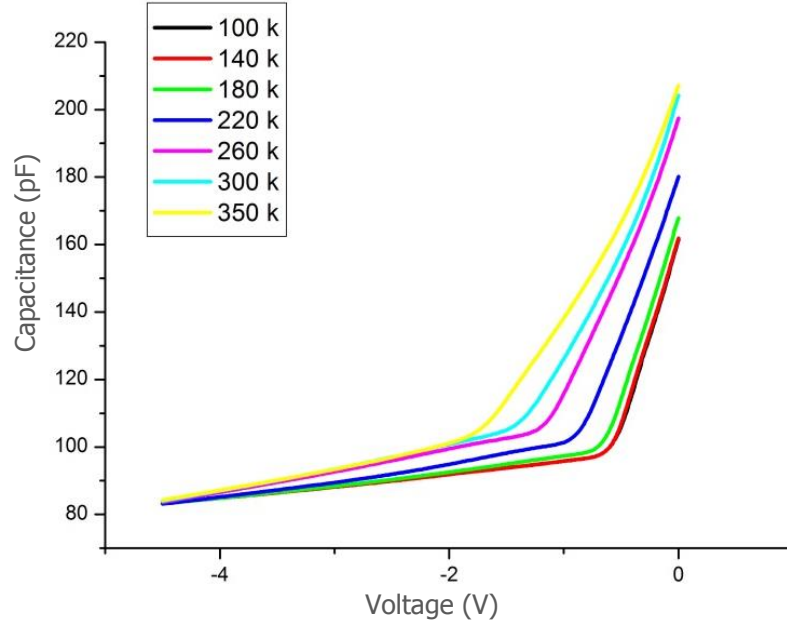


Fig. 4.16: C-V curve for ASN3464 at different temperature. The site-controlled QDs layer is grown on top.

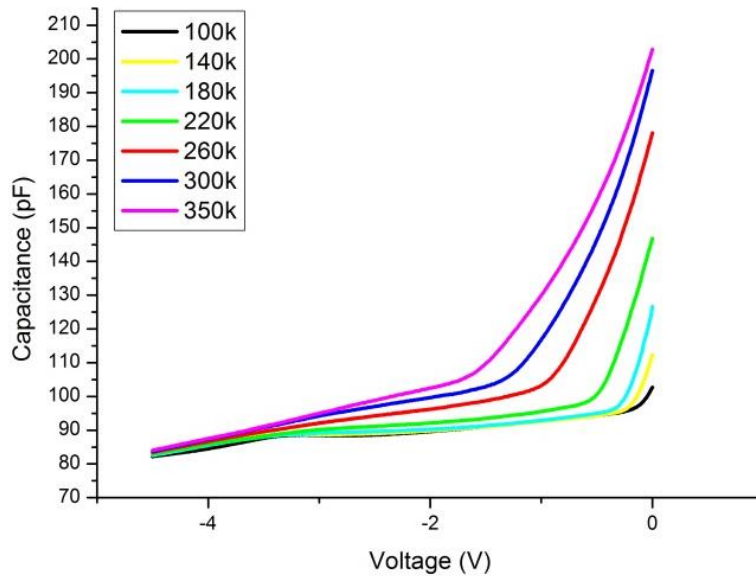


Fig. 4.17: C-V curve for ASN3464 at different temperature. The site-controlled QDs layer is grown on top. Measurements are done in the unpatterned area,

Finally, in order to sum up the results, figure 4.18 shows the C-V curve for the samples at room temperature. It is noticed that the sample in which the sample having only re-growth interfaces seems reasonably fine. However, once the samples are chemically cleaned the defects starts to strongly affect the capacitance. Increasing the reverse bias voltage should increase the depletion region. However due to the defects from the chemical cleaning, the electrons are trapped and do not contribute to the capacitance.

After certain reverse bias, the depletion region gets wider and passes over the defects layer. The capacitance behaviour is normal again.

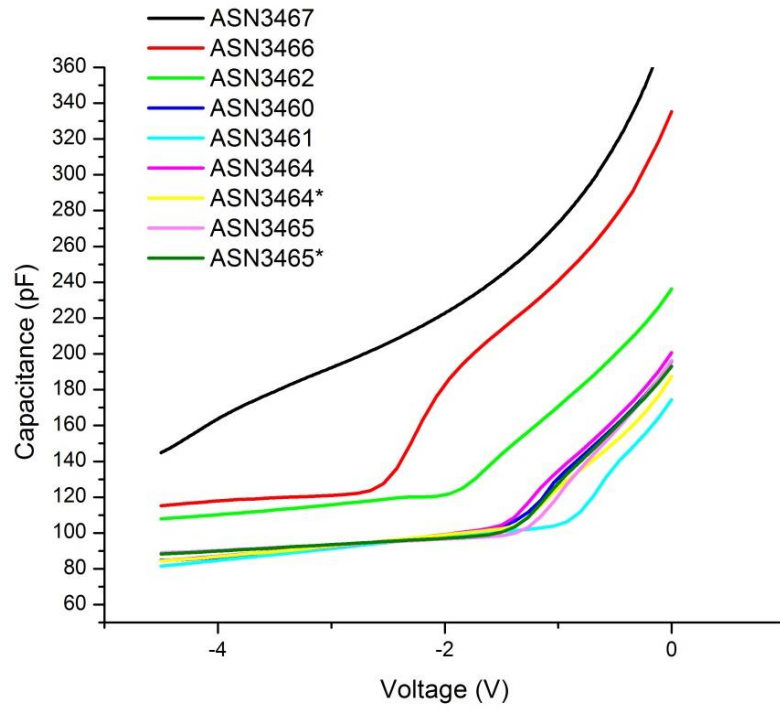


Fig. 4.18: C-V measurements for all samples at room temperature. It shows that once the samples are chemically cleaned before loading it to the MBE reactor, a remarkable defects layer rises and keeps the depletion layer from expanding until a certain value of reverse bias is applied.

5. CONCLUSION

The aim of the thesis is to characterize the InAs/GaAs site-controlled QDs electrically and to study its surface properties as well. Being part of the PhotonicQCA project, the surface characterization focused on the measurements of the double QDs spacing using AFM and SEM techniques. The study starts with selecting the suitable diameter of the pit. The selected diameter had to give the highest probability not only to be filled but also to be filled with one QD. The suitable diameter was 50 nm. Additionally, different orientation for the double pits has been used; [011], [0-11] and [010]. The surface study of the double QDs shows that the [011] double QDs should be the most suitable candidate to fulfil the requirements of having a Photonic QCA. The [011] can be used to obtain the minimum spacing between the QDs. Additionally, the spacing between the QDs increases steadily with the increase of the distance between the two QDs. The [0-11] double QDs remained merged until the spacing between the two QDs is around 90 nm. On the same hand, for the [010] double QDs; it was found that the spacing between the QDs increases rapidly when the distance between them is slightly increased. Thus, it will not be easy to control the distance between them.

Regarding, the electrical characterization, a Schottky diode structure with a site-controlled QDs layer embedded inside has been studied. The C-V measurements are performed for 9 different samples in order to show the effect of each fabrication step on the capacitance as a function of the applied reverse voltage. The depletion region changes relatively with the applied voltage. Electrons are trapped and then the QDs get empty depending on the location of the depletion region. Unfortunately, the chemical cleaning step which is always required before the sample is loaded to the MBE reactor creates a remarkable defects layer which degrades the overall capacitance and keeps the electrons trapped until the reverse voltage is remarkably high.

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APPENDIX I

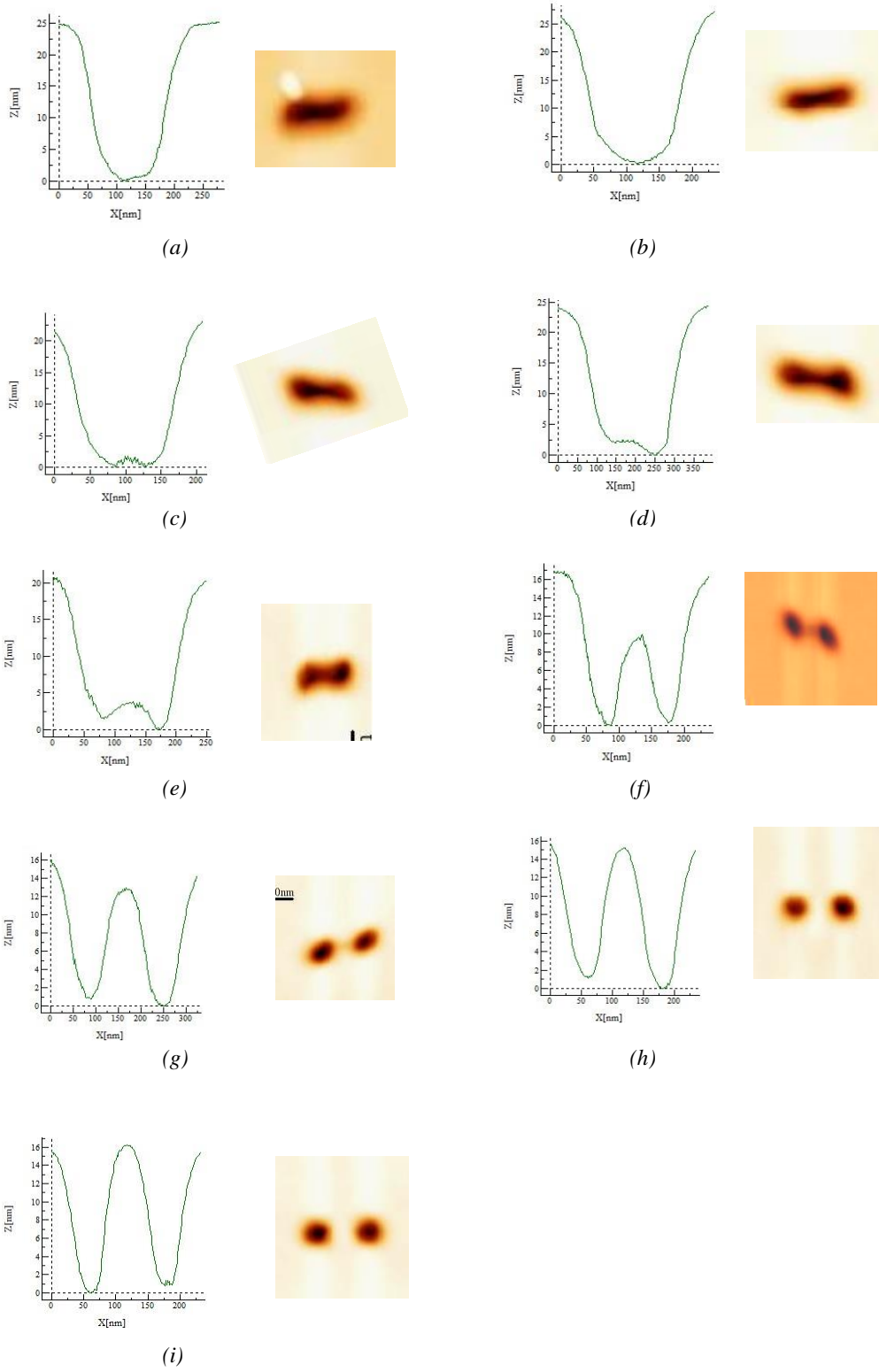


Fig. 1: HDP study at different spacing; (a) 45 nm (b) 50 nm (c) 55 nm (d) 60 nm (e) 65 nm (f) 70 nm (g) 80 nm (h) 90 nm (i) 100 nm.

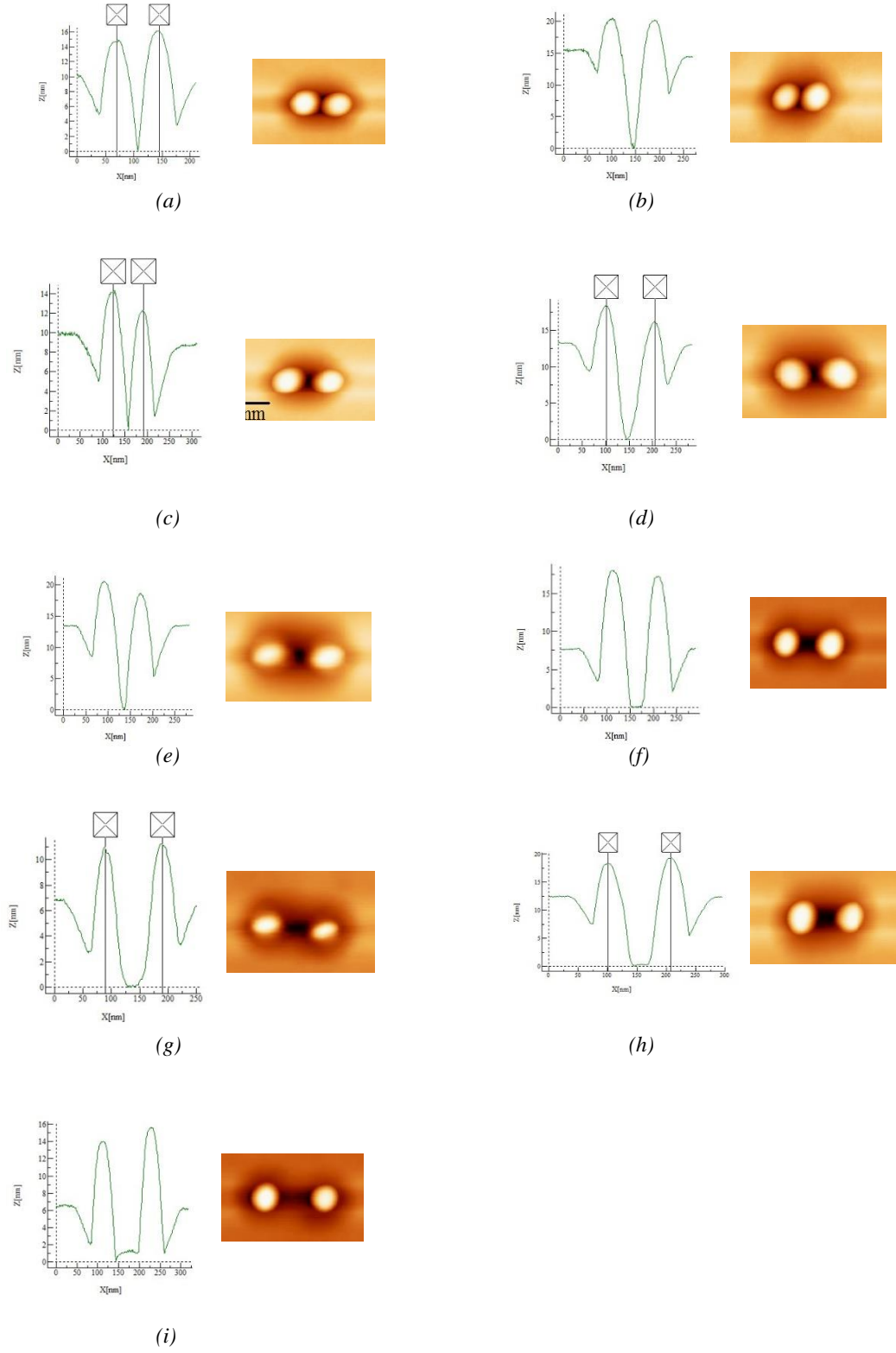


Fig. 2: HDP study after they are occupied with the QDs at different spacing; (a) 45 nm (b) 50 nm (c) 55 nm (d) 60 nm (e) 65 nm (f) 70 nm (g) 80 nm (h) 90 nm (i) 100 nm.

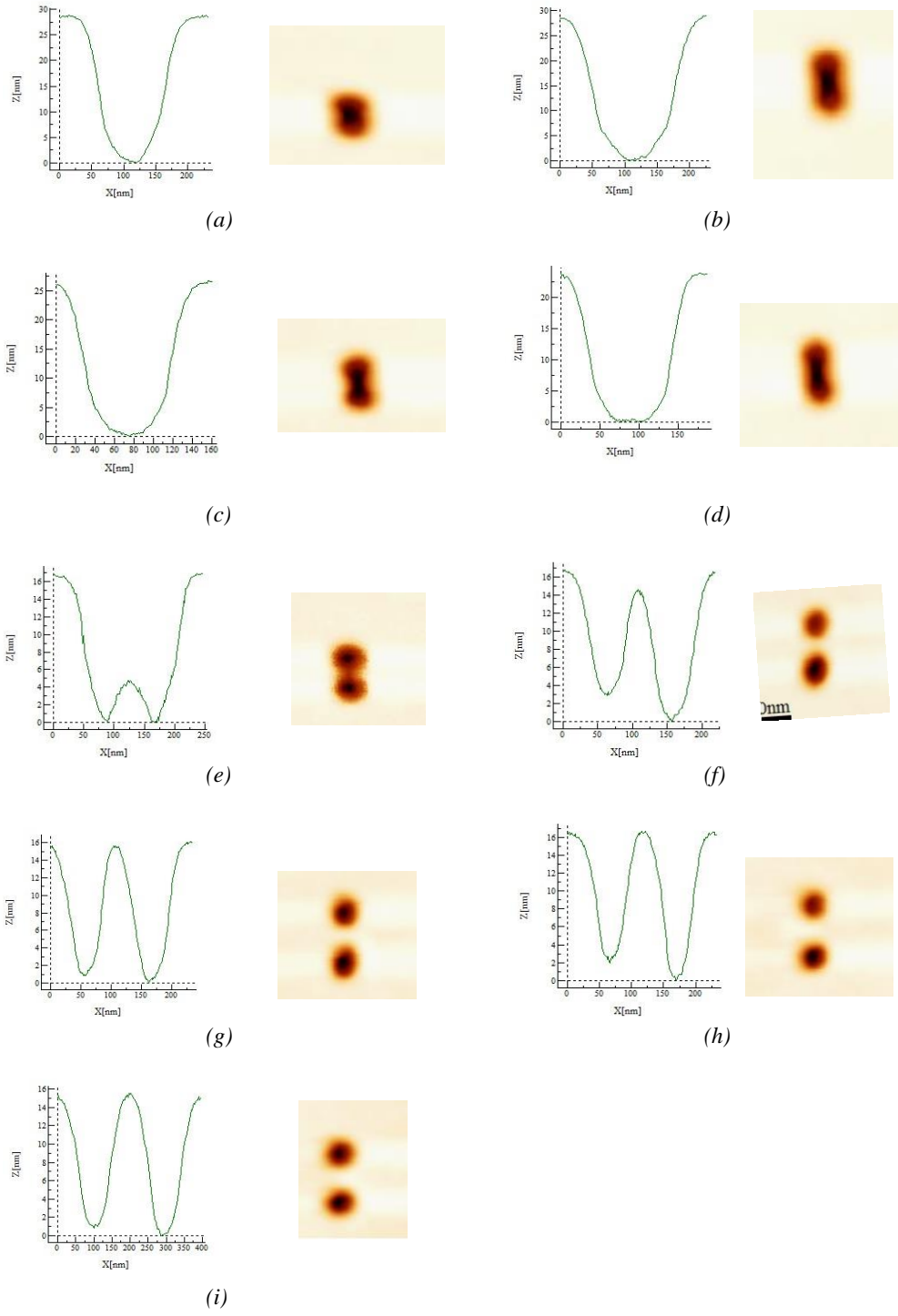


Fig. 3: VDP study at different spacing; (a) 45 nm (b) 50 nm (c) 55 nm (d) 60 nm (e) 65 nm (f) 70 nm (g) 80 nm (h) 90 nm (i) 100 nm.

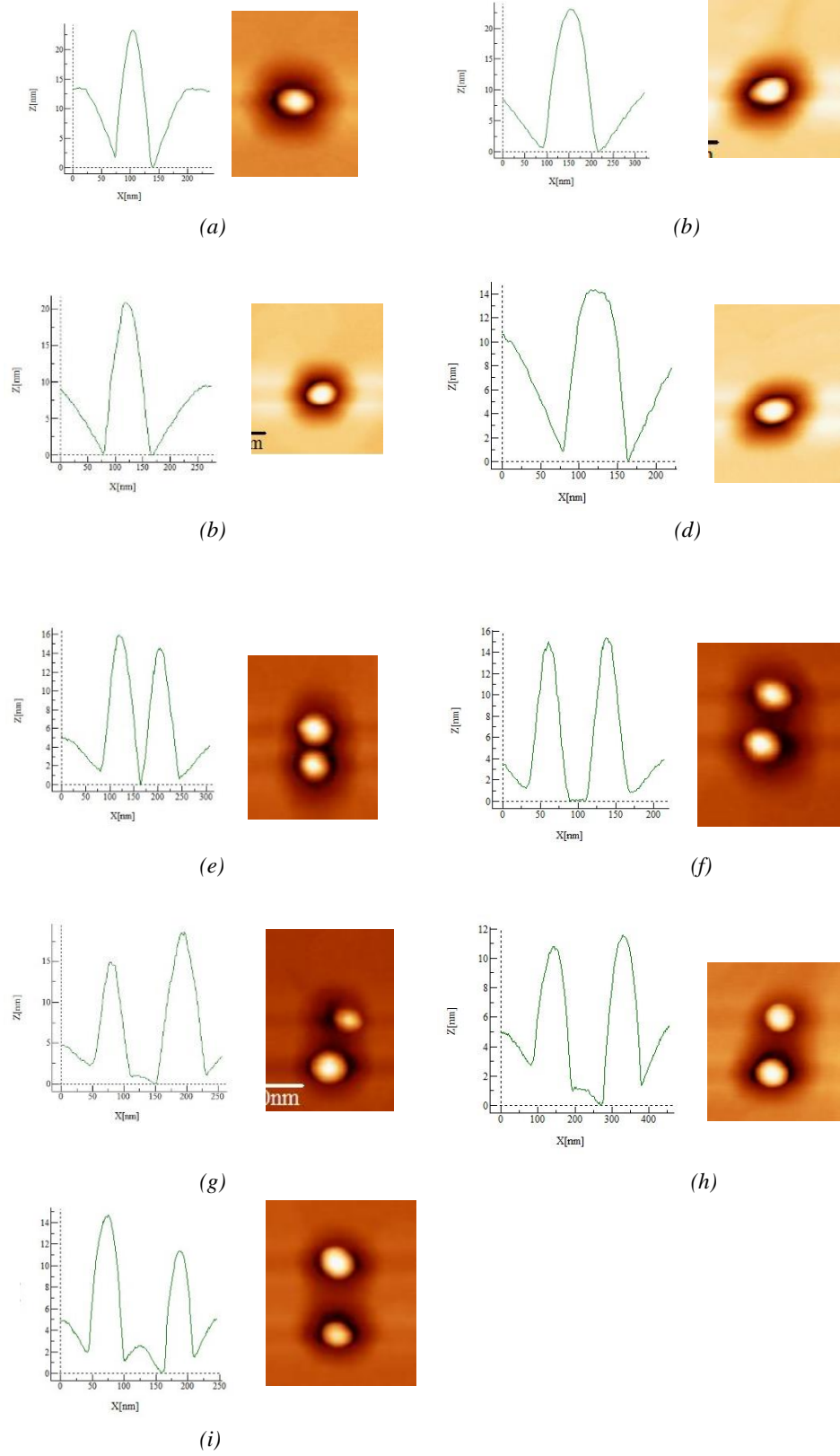


Fig. 4: VDP study after they are occupied with the QDs at different spacing; (a) 45 nm (b) 50 nm (c) 55 nm (d) 60 nm (e) 65 nm (f) 70 nm (g) 80 nm (h) 90 nm (i) 100 nm.

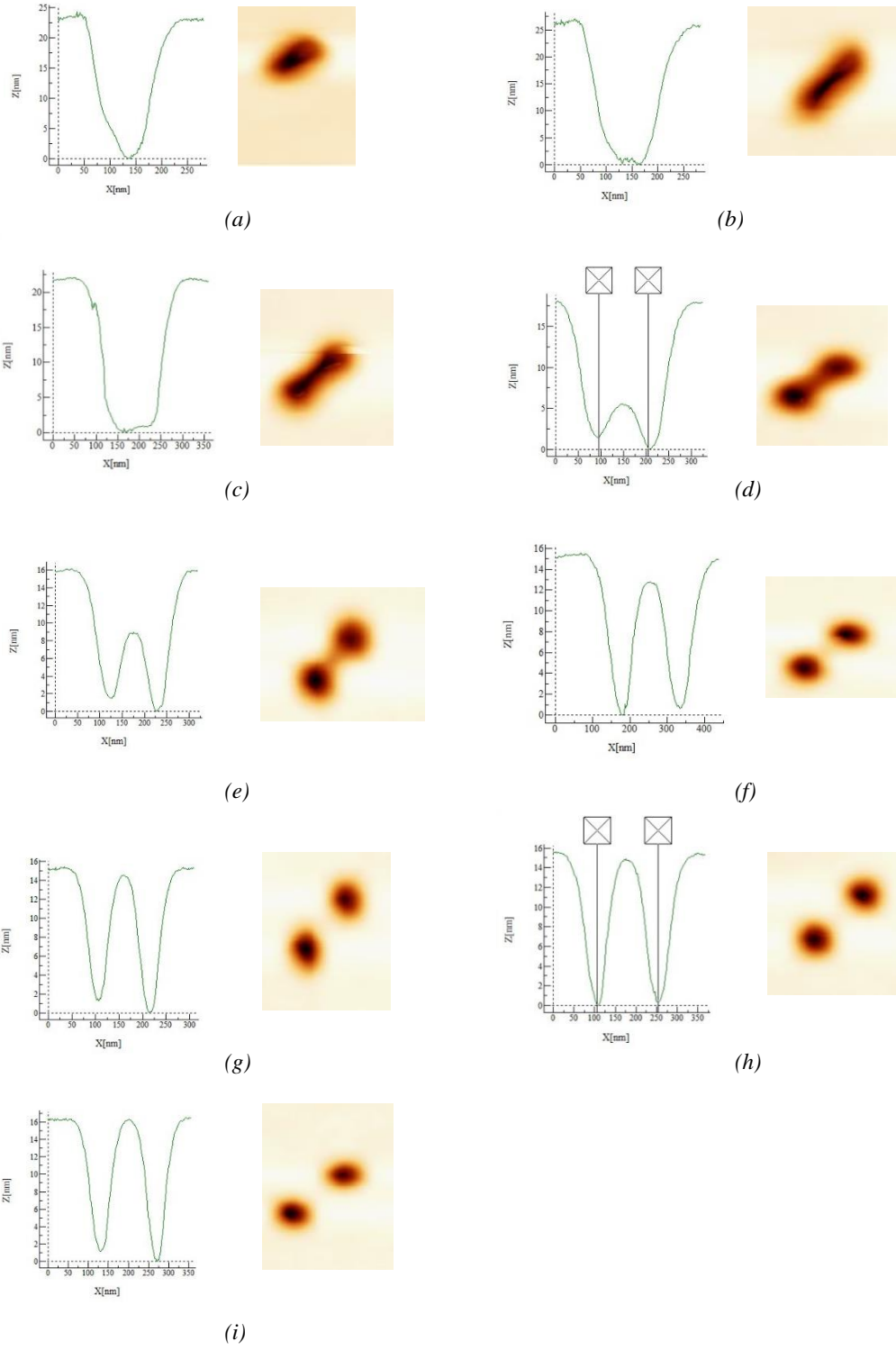


Fig. 5: CDP study at different spacing; (a) 42 nm (b) 50 nm (c) 57 nm (d) 65 nm (e) 71 nm (f) 78 nm (g) 85 nm (h) 92 nm (i) 100 nm .

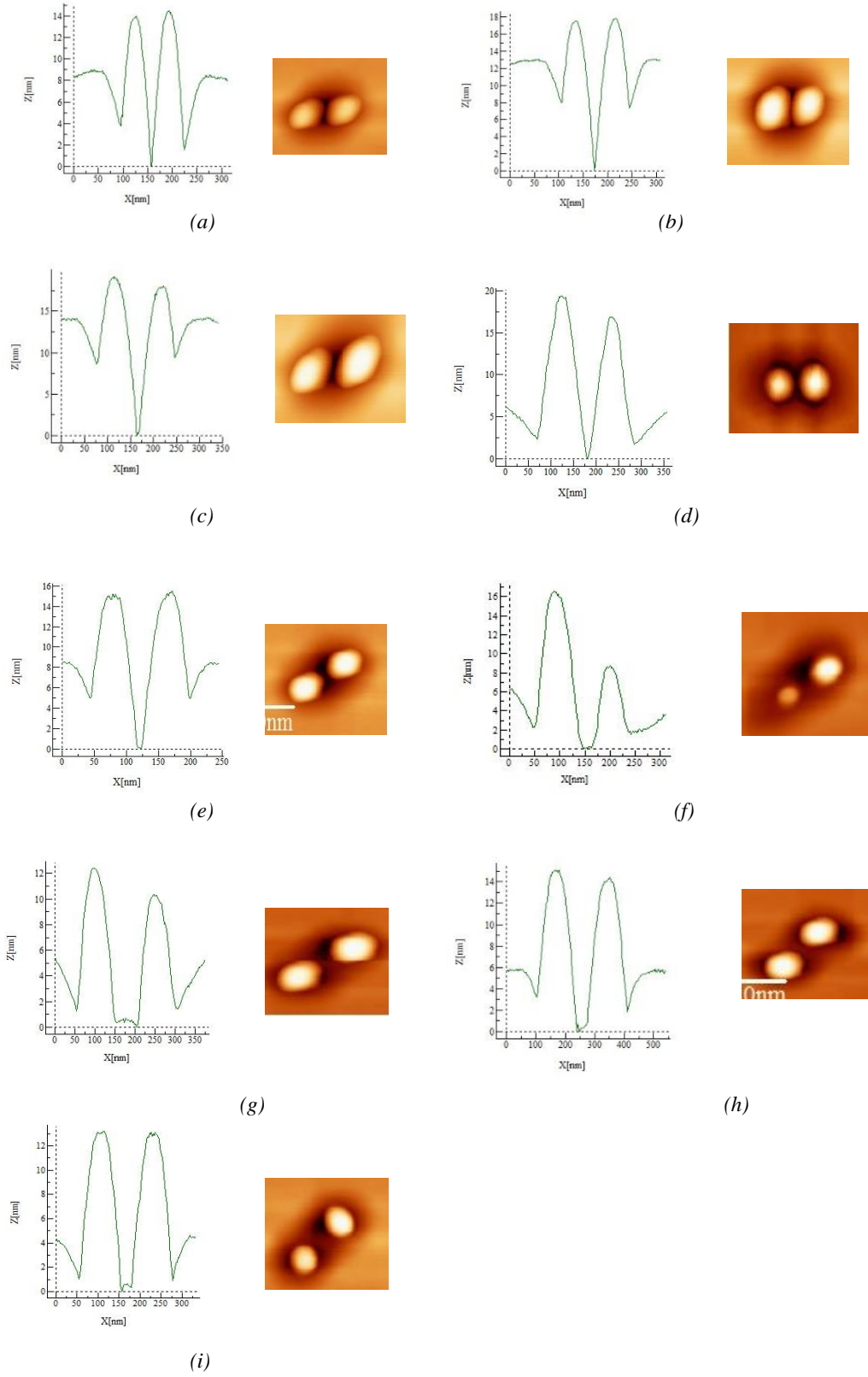


Fig. 6: CDP study after they are occupied with the QDs at different spacing; (a) 42 nm (b) 50 nm (c) 57 nm (d) 65 nm (e) 71 nm (f) 78 nm (g) 85 nm (h) 92 nm (i) 100 nm.